FIG.1

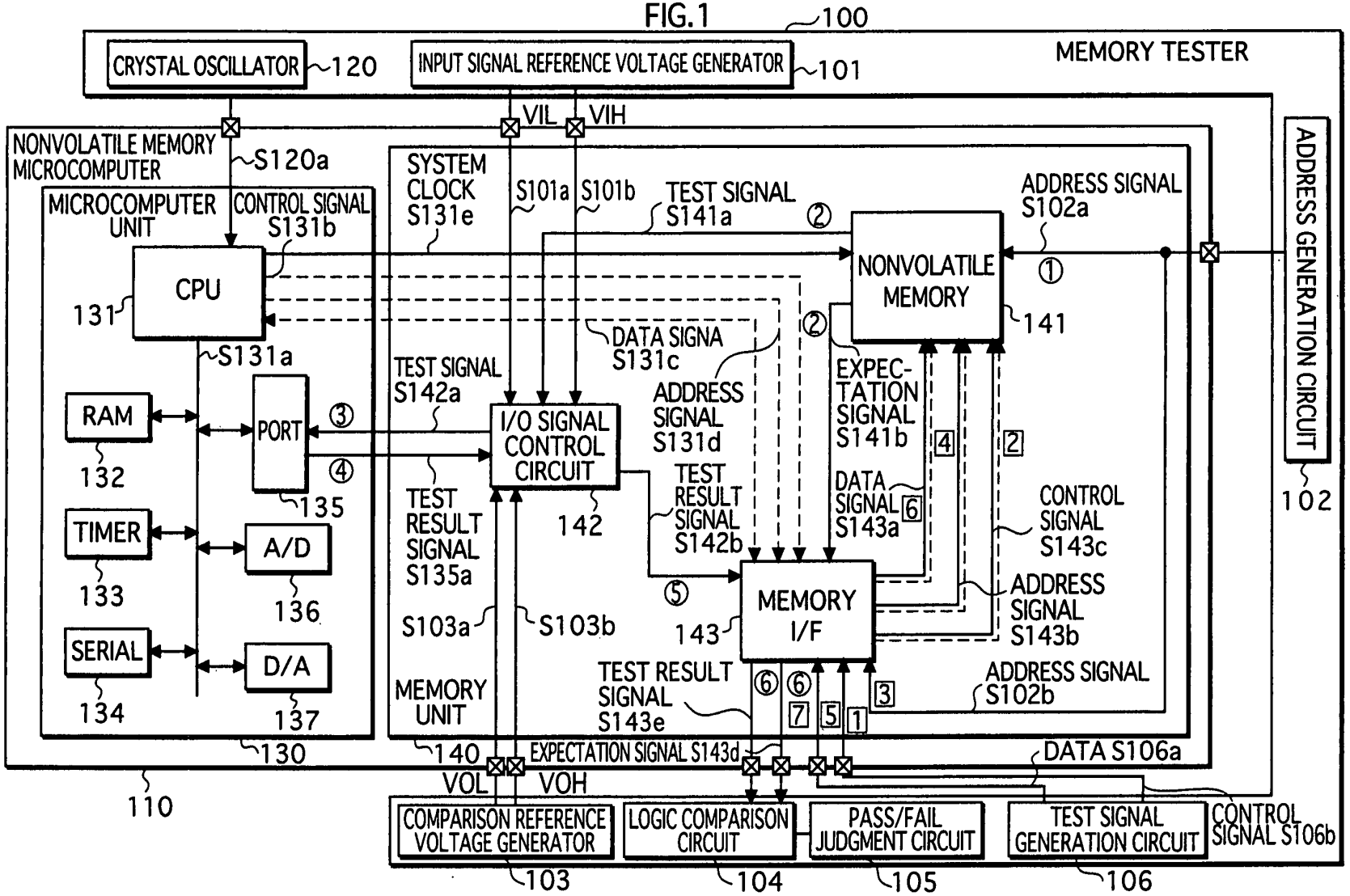

100
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
CPU
131
S131a
RAM
132
TIMER
133
SERIAL
134
PORT
135
A/D
136
D/A
137
130
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
ADDRESS SIGNAL S102a
NONVOLATILE MEMORY
141
DATA SIGNA S131c
EXPEC-TATION SIGNAL S141b
TEST SIGNAL S142a
I/O SIGNAL CONTROL CIRCUIT
142
ADDRESS SIGNAL S131d
TEST RESULT SIGNAL S135a
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
ADDRESS SIGNAL S143b
MEMORY I/F
143
S103a
S103b
MEMORY UNIT
140
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL S102b
EXPECTATION SIGNAL S143d
DATA S106a
VOL
VOH
110
COMPARISON REFERENCE VOLTAGE GENERATOR
103
LOGIC COMPARISON CIRCUIT
104
PASS/FAIL JUDGMENT CIRCUIT
105
TEST SIGNAL GENERATION CIRCUIT
106
CONTROL SIGNAL S106b
ADDRESS GENERATION CIRCUIT
102

FIG.2

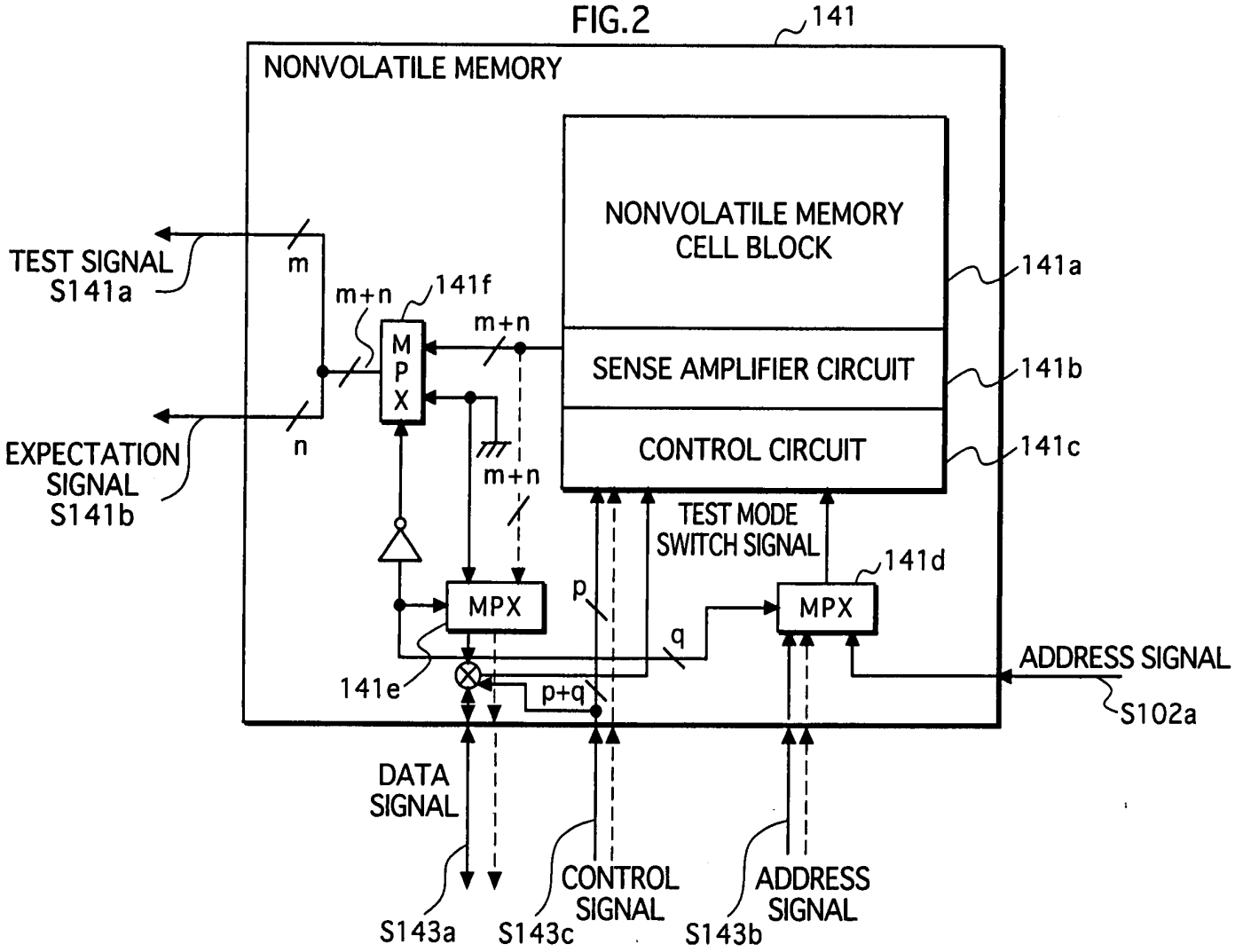

141
NONVOLATILE MEMORY
NONVOLATILE MEMORY CELL BLOCK
141a
SENSE AMPLIFIER CIRCUIT
141b
CONTROL CIRCUIT
141c
TEST SIGNAL S141a
EXPECTATION SIGNAL S141b
m
n
m+n
141f
MPX
m+n
m+n
TEST MODE SWITCH SIGNAL
141d
MPX
MPX
p
q
141e
p+q
ADDRESS SIGNAL
S102a
DATA SIGNAL
CONTROL SIGNAL
ADDRESS SIGNAL
S143a
S143c
S143b

FIG.3

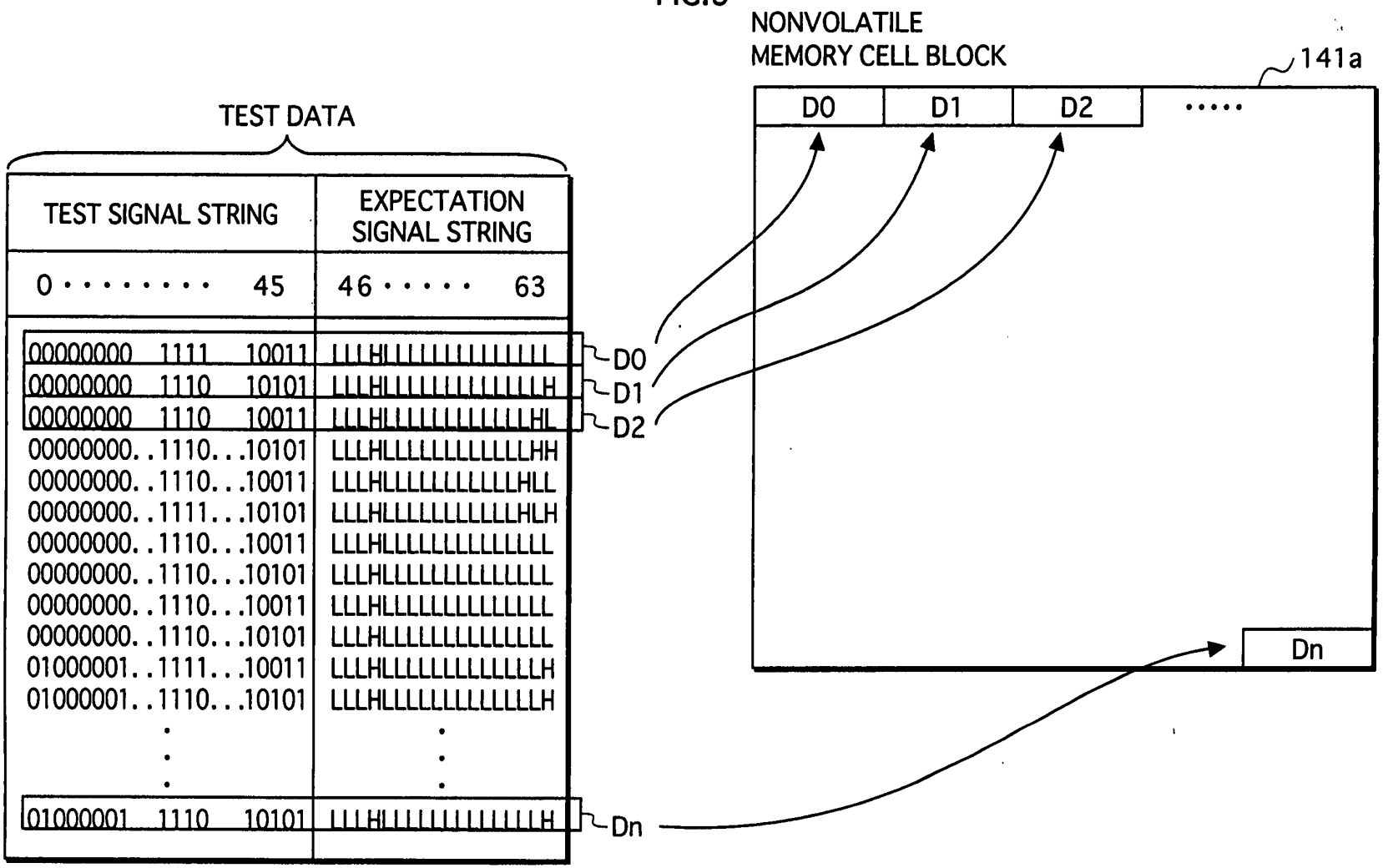

TEST DATA
TEST SIGNAL STRING
EXPECTATION SIGNAL STRING
0 ・・・・・・・・ 45
46 ・・・・・ 63
00000000 1111 10011 LLLHLLLLLLLLLLLLL
00000000 1110 10101 LLLHLLLLLLLLLLLLH
00000000 1110 10011 LLLHLLLLLLLLLLLHL
00000000..1110...10101 LLLHLLLLLLLLLLLHH
00000000..1110...10011 LLLHLLLLLLLLLLHLL
00000000..1111...10101 LLLHLLLLLLLLLLHLH
00000000..1110...10011 LLLHLLLLLLLLLLLLL
00000000..1110...10101 LLLHLLLLLLLLLLLLL
00000000..1110...10011 LLLHLLLLLLLLLLLLL
00000000..1110...10101 LLLHLLLLLLLLLLLLL
01000001..1111...10011 LLLHLLLLLLLLLLLLH
01000001..1110...10101 LLLHLLLLLLLLLLLLH
01000001 1110 10101 LLLHLLLLLLLLLLLLH
D0
D1
D2
Dn
NONVOLATILE MEMORY CELL BLOCK
141a
D0
D1
D2
・・・・・
Dn

FIG.4

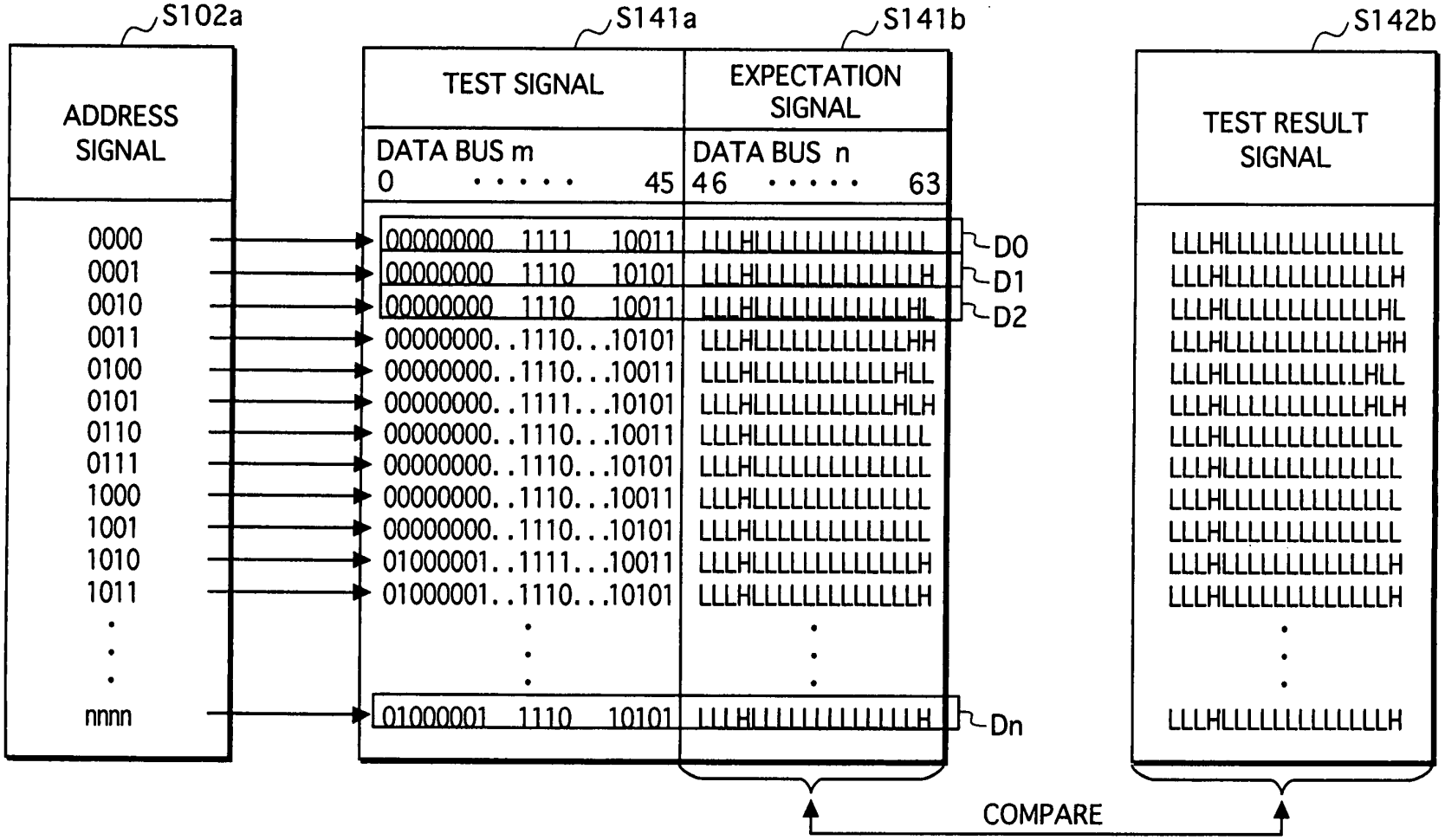

S102a
S141a
S141b
S142b
ADDRESS SIGNAL
TEST SIGNAL
EXPECTATION SIGNAL
TEST RESULT SIGNAL
DATA BUS m
0 • • • • • 45
DATA BUS n
46 • • • • • 63
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
nnnn
00000000 1111 10011 LLLHLLLLLLLLLLLL
00000000 1110 10101 LLLHLLLLLLLLLLLH
00000000 1110 10011 LLLHLLLLLLLLLLHL
00000000..1110...10101 LLLHLLLLLLLLLLHH
00000000..1110...10011 LLLHLLLLLLLLLHLL
00000000..1111...10101 LLLHLLLLLLLLLHLH
00000000..1110...10011 LLLHLLLLLLLLLLLL
00000000..1110...10101 LLLHLLLLLLLLLLLL
00000000..1110...10011 LLLHLLLLLLLLLLLL
00000000..1110...10101 LLLHLLLLLLLLLLLL
01000001..1111...10011 LLLHLLLLLLLLLLLH
01000001..1110...10101 LLLHLLLLLLLLLLLH
01000001 1110 10101 LLLHLLLLLLLLLLLH
D0
D1
D2
Dn
COMPARE

FIG.5

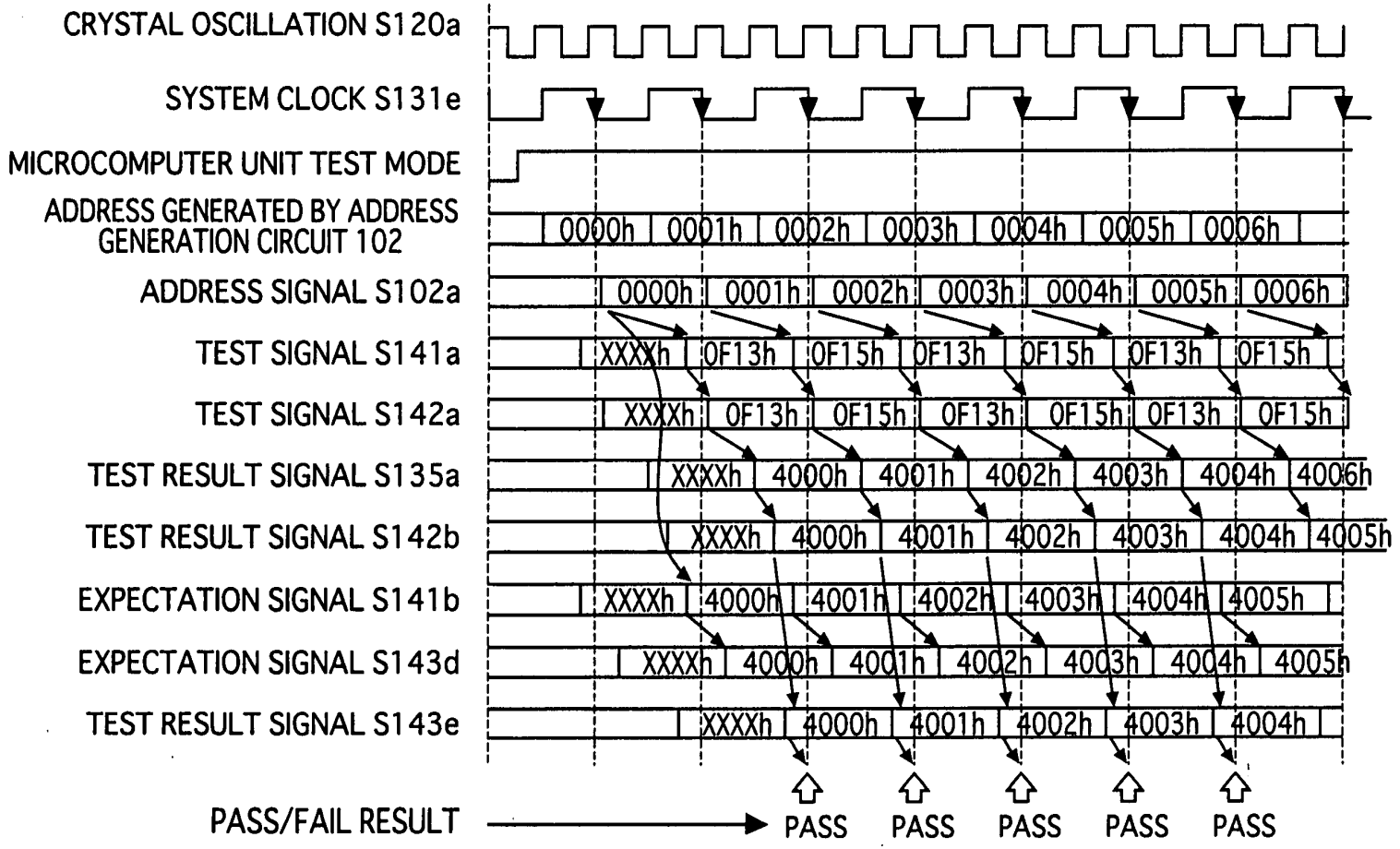

CRYSTAL OSCILLATION S120a
SYSTEM CLOCK S131e
MICROCOMPUTER UNIT TEST MODE
ADDRESS GENERATED BY ADDRESS GENERATION CIRCUIT 102
0000h 0001h 0002h 0003h 0004h 0005h 0006h
ADDRESS SIGNAL S102a
0000h 0001h 0002h 0003h 0004h 0005h 0006h
TEST SIGNAL S141a
XXXXh 0F13h 0F15h 0F13h 0F15h 0F13h 0F15h
TEST SIGNAL S142a
XXXXh 0F13h 0F15h 0F13h 0F15h 0F13h 0F15h
TEST RESULT SIGNAL S135a
XXXXh 4000h 4001h 4002h 4003h 4004h 4006h
TEST RESULT SIGNAL S142b
XXXXh 4000h 4001h 4002h 4003h 4004h 4005h
EXPECTATION SIGNAL S141b
XXXXh 4000h 4001h 4002h 4003h 4004h 4005h
EXPECTATION SIGNAL S143d
XXXXh 4000h 4001h 4002h 4003h 4004h 4005h
TEST RESULT SIGNAL S143e
XXXXh 4000h 4001h 4002h 4003h 4004h
PASS/FAIL RESULT
PASS PASS PASS PASS PASS

FIG.6

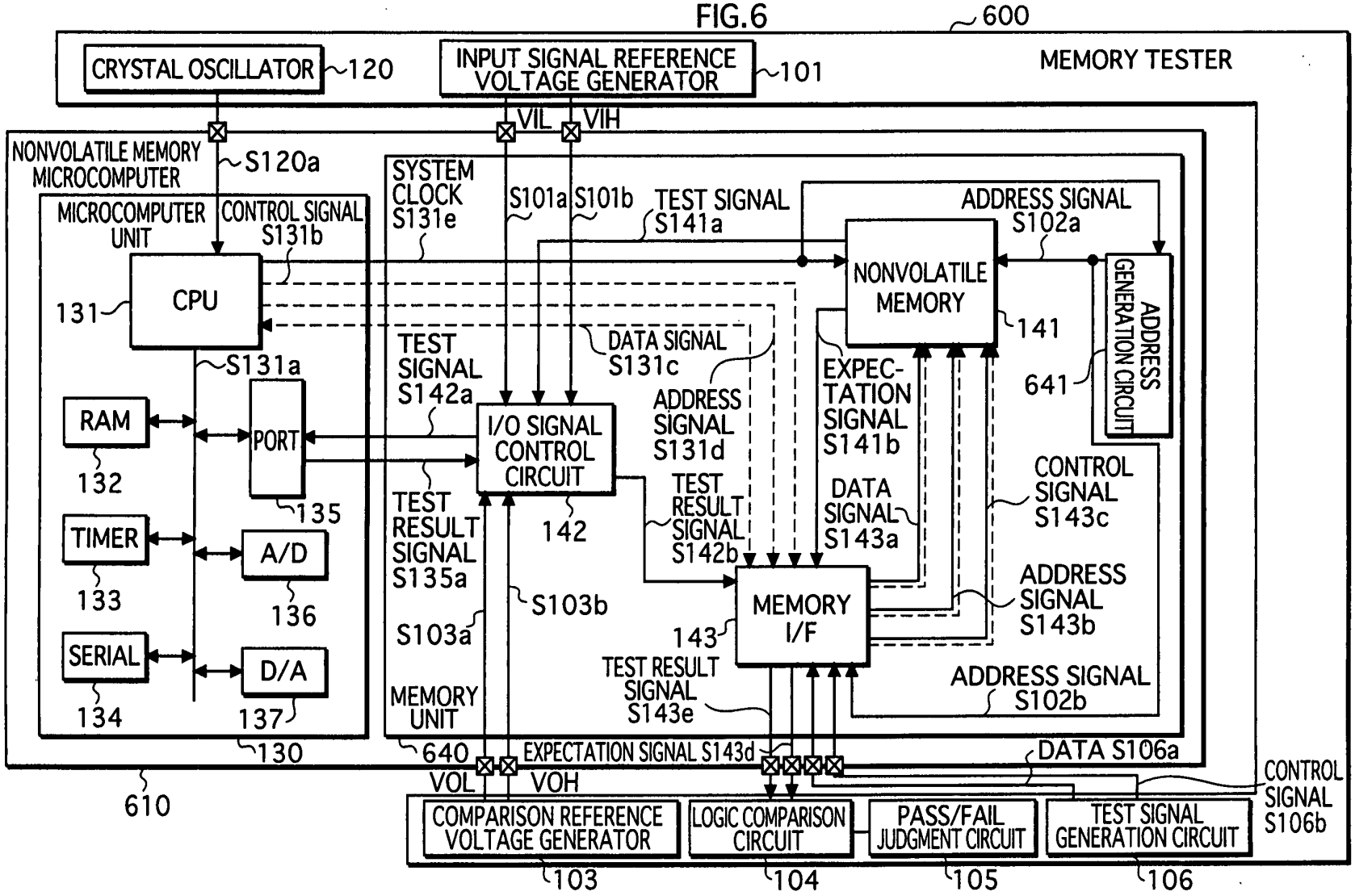

600
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
CPU
131
S131a
RAM
132
PORT
135
TIMER
133
A/D
136
SERIAL
134
D/A
137
130
610
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
ADDRESS SIGNAL S102a
NONVOLATILE MEMORY
141
ADDRESS GENERATION CIRCUIT
641
TEST SIGNAL S142a
DATA SIGNAL S131c
ADDRESS SIGNAL S131d
EXPEC-TATION SIGNAL S141b
I/O SIGNAL CONTROL CIRCUIT
142
TEST RESULT SIGNAL S135a
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
S103a
S103b
MEMORY I/F
143
ADDRESS SIGNAL S143b
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL S102b
MEMORY UNIT
640
EXPECTATION SIGNAL S143d
DATA S106a
VOL
VOH
CONTROL SIGNAL S106b
COMPARISON REFERENCE VOLTAGE GENERATOR
103
LOGIC COMPARISON CIRCUIT
104
PASS/FAIL JUDGMENT CIRCUIT
105
TEST SIGNAL GENERATION CIRCUIT
106

FIG.7

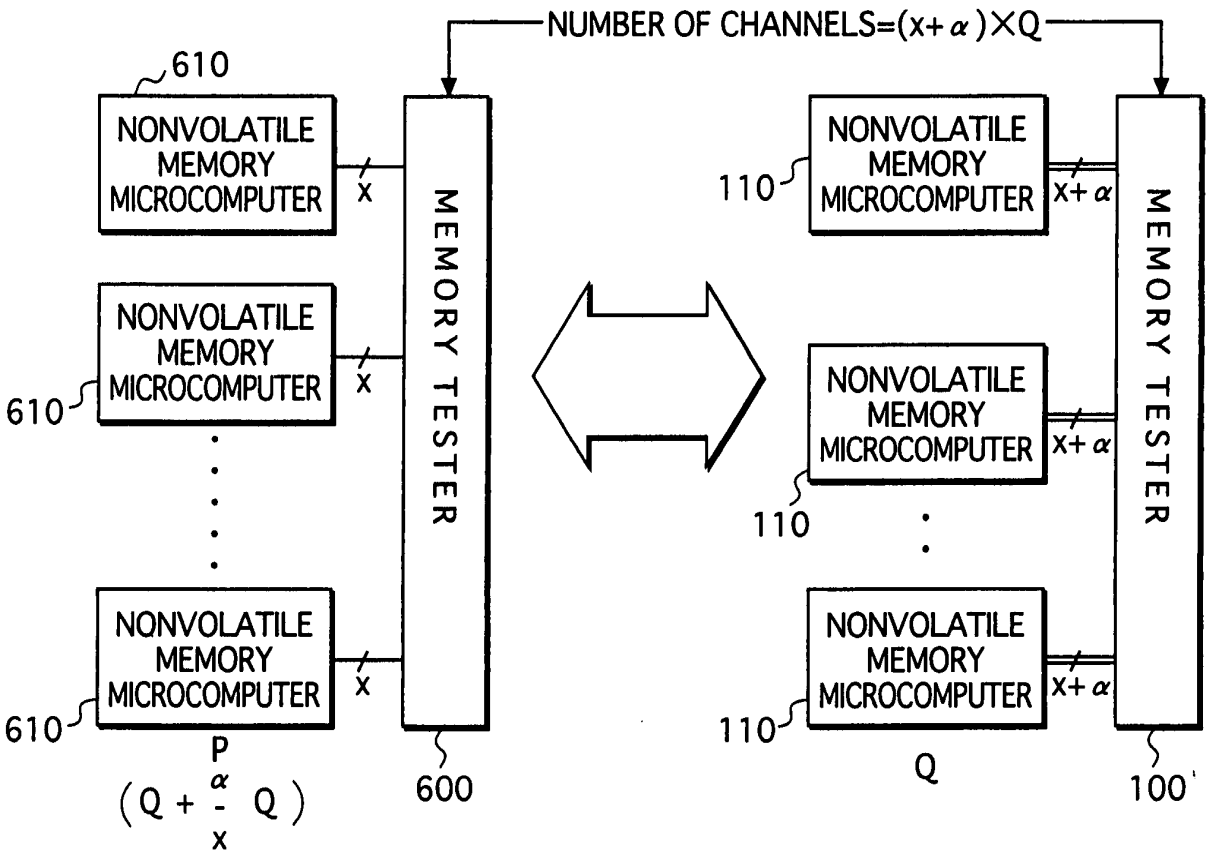

NUMBER OF CHANNELS=(x+α)×Q
610
NONVOLATILE MEMORY MICROCOMPUTER
x
MEMORY TESTER
610
610
P
(Q + α/x Q)
600
110
x+α
110
110
Q
100

FIG.8

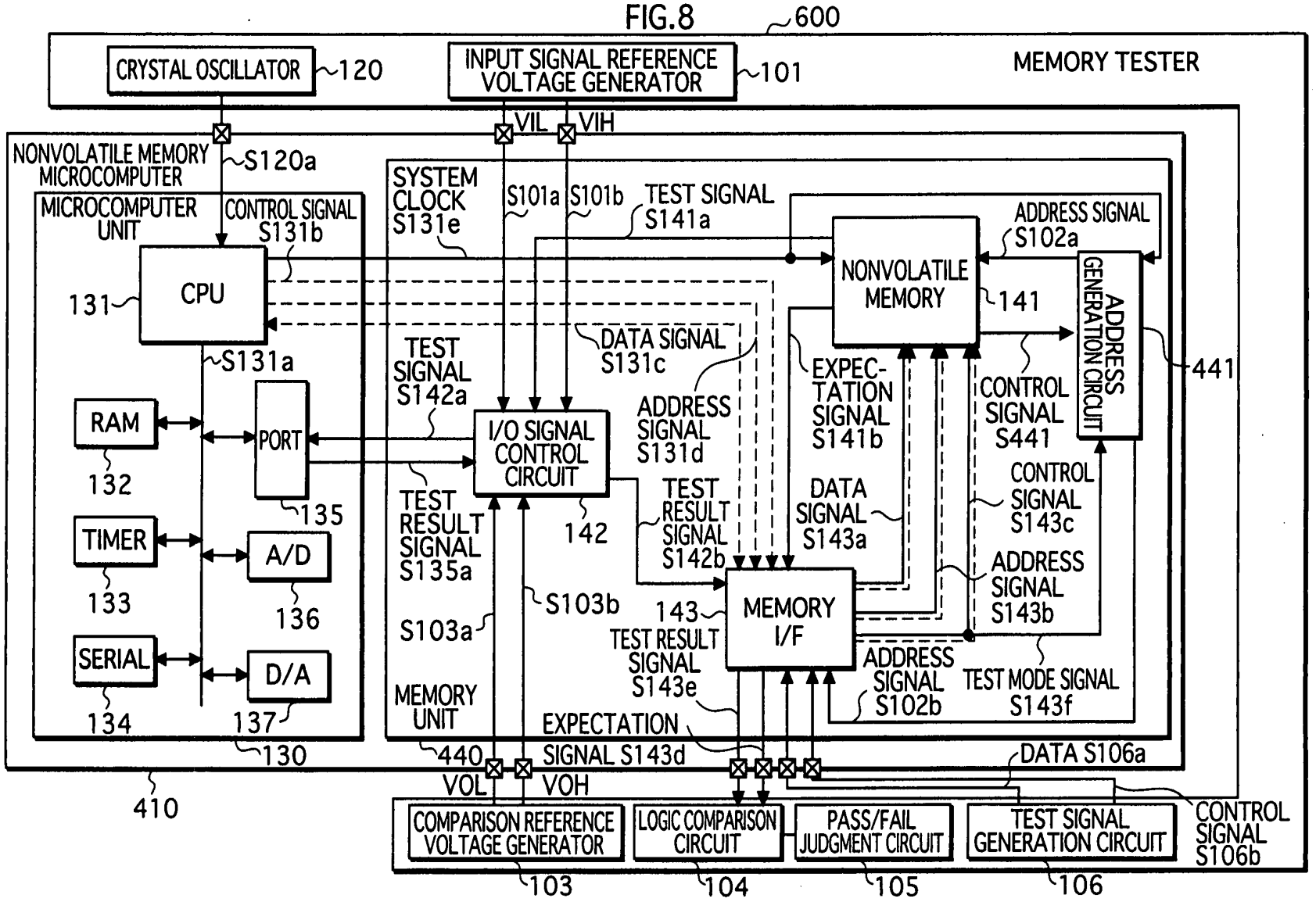

600
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
CPU
131
S131a
RAM
132
PORT
135
TIMER
133
A/D
136
SERIAL
134
D/A
137
130
410
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
ADDRESS SIGNAL S102a
NONVOLATILE MEMORY
141
ADDRESS GENERATION CIRCUIT
441
DATA SIGNAL S131c
TEST SIGNAL S142a
I/O SIGNAL CONTROL CIRCUIT
142
ADDRESS SIGNAL S131d
EXPEC-TATION SIGNAL S141b
CONTROL SIGNAL S441
TEST RESULT SIGNAL S135a
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
S103a
S103b
143
MEMORY I/F
ADDRESS SIGNAL S143b
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL S102b
TEST MODE SIGNAL S143f
MEMORY UNIT
EXPECTATION SIGNAL S143d
440
DATA S106a
VOL
VOH
CONTROL SIGNAL S106b
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
103
104
105
106

FIG.9

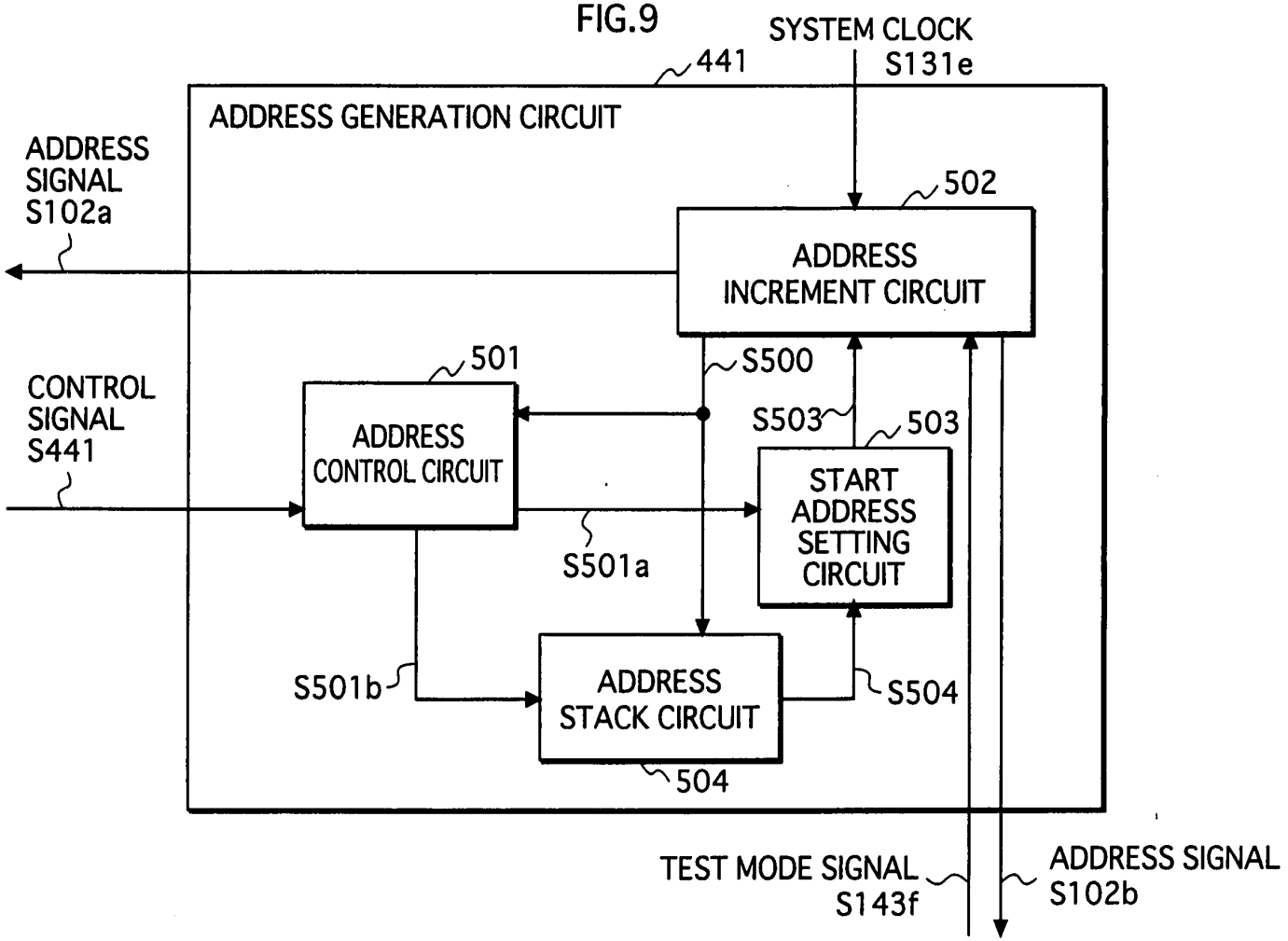

441
SYSTEM CLOCK
S131e
ADDRESS GENERATION CIRCUIT
ADDRESS
SIGNAL
S102a
502
ADDRESS
INCREMENT CIRCUIT
501
S500
CONTROL
SIGNAL
S441
ADDRESS
CONTROL CIRCUIT
S503
503
START
ADDRESS
SETTING
CIRCUIT
S501a
S501b
ADDRESS
STACK CIRCUIT
S504
504
TEST MODE SIGNAL
S143f
ADDRESS SIGNAL
S102b

FIG.10

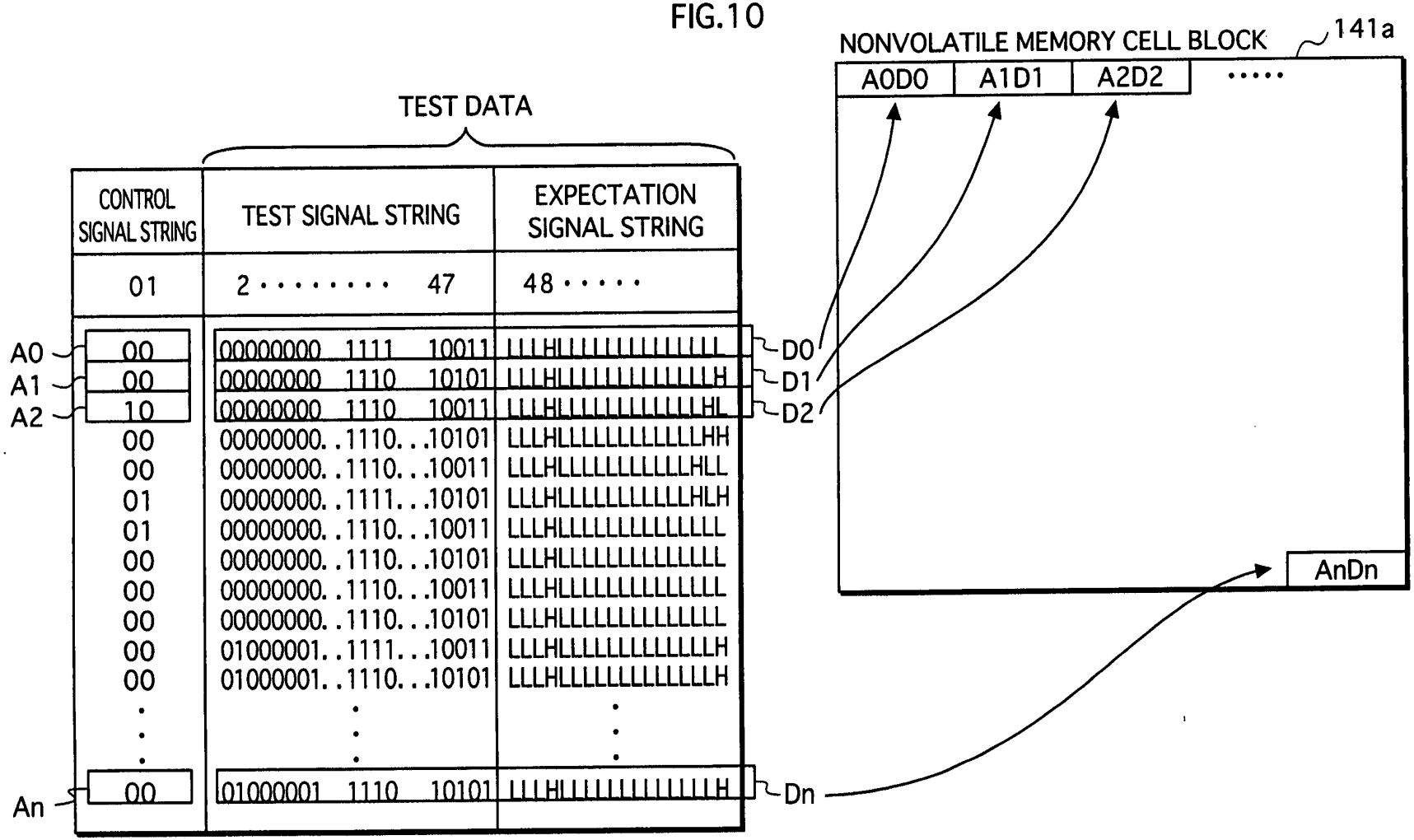

TEST DATA
CONTROL SIGNAL STRING
TEST SIGNAL STRING
EXPECTATION SIGNAL STRING
01
2 ····· 47
48 ·····
A0
A1
A2
An
00
00
10
00
00
01
01
00
00
00
00
00
00
00000000 1111 10011
00000000 1110 10101
00000000 1110 10011
00000000..1110...10101
00000000..1110...10011
00000000..1111...10101
00000000..1110...10011
00000000..1110...10101
00000000..1110...10011
00000000..1110...10101
01000001..1111...10011
01000001..1110...10101
01000001 1110 10101
LLLHLLLLLLLLLLLL
LLLHLLLLLLLLLLLLH
LLLHLLLLLLLLLLLLHL
LLLHLLLLLLLLLLLLHH
LLLHLLLLLLLLLLLLHLL
LLLHLLLLLLLLLLLLHLH
LLLHLLLLLLLLLLLLL
LLLHLLLLLLLLLLLLL
LLLHLLLLLLLLLLLLL
LLLHLLLLLLLLLLLLL
LLLHLLLLLLLLLLLLLH
LLLHLLLLLLLLLLLLLH
LLLHLLLLLLLLLLLLLH
D0
D1
D2
Dn
NONVOLATILE MEMORY CELL BLOCK
141a
A0D0
A1D1
A2D2
·····
AnDn

FIG.11

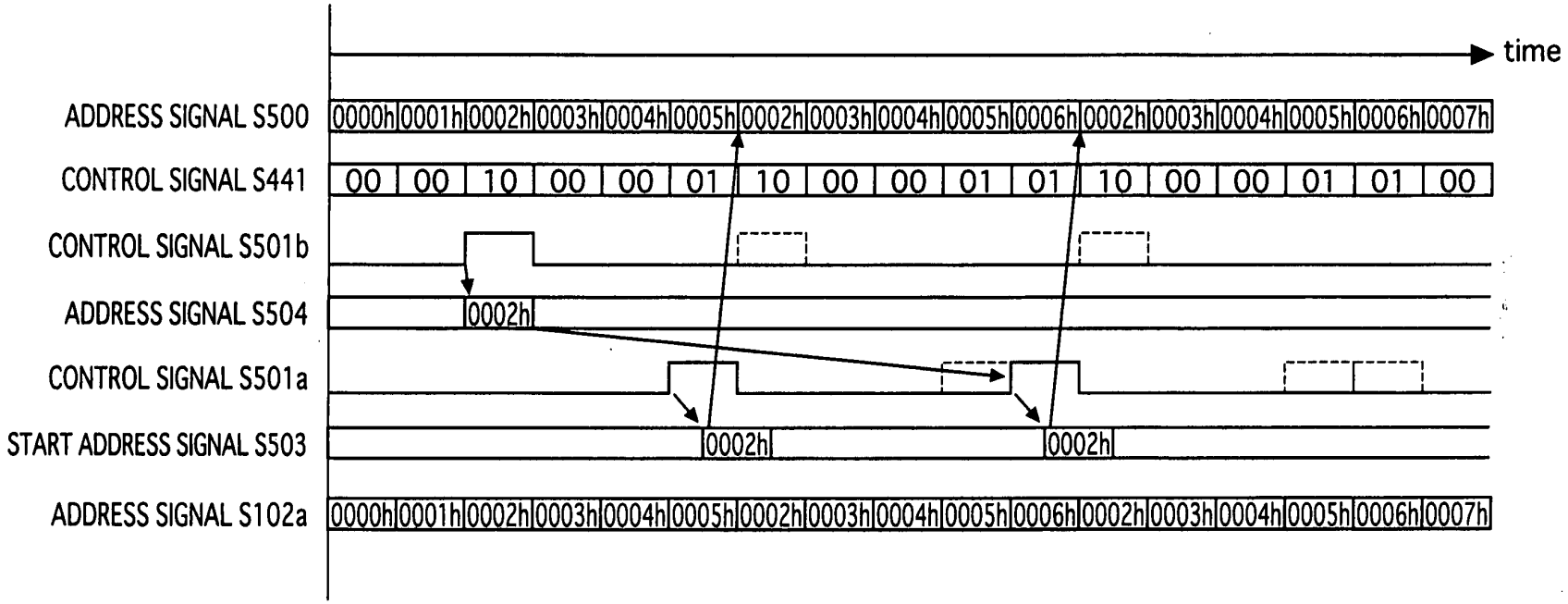

time
ADDRESS SIGNAL S500
0000h 0001h 0002h 0003h 0004h 0005h 0002h 0003h 0004h 0005h 0006h 0002h 0003h 0004h 0005h 0006h 0007h
CONTROL SIGNAL S441
00 00 10 00 00 01 10 00 00 01 01 10 00 00 01 01 00
CONTROL SIGNAL S501b
ADDRESS SIGNAL S504
0002h
CONTROL SIGNAL S501a
START ADDRESS SIGNAL S503
0002h
0002h
ADDRESS SIGNAL S102a
0000h 0001h 0002h 0003h 0004h 0005h 0002h 0003h 0004h 0005h 0006h 0002h 0003h 0004h 0005h 0006h 0007h

FIG.12

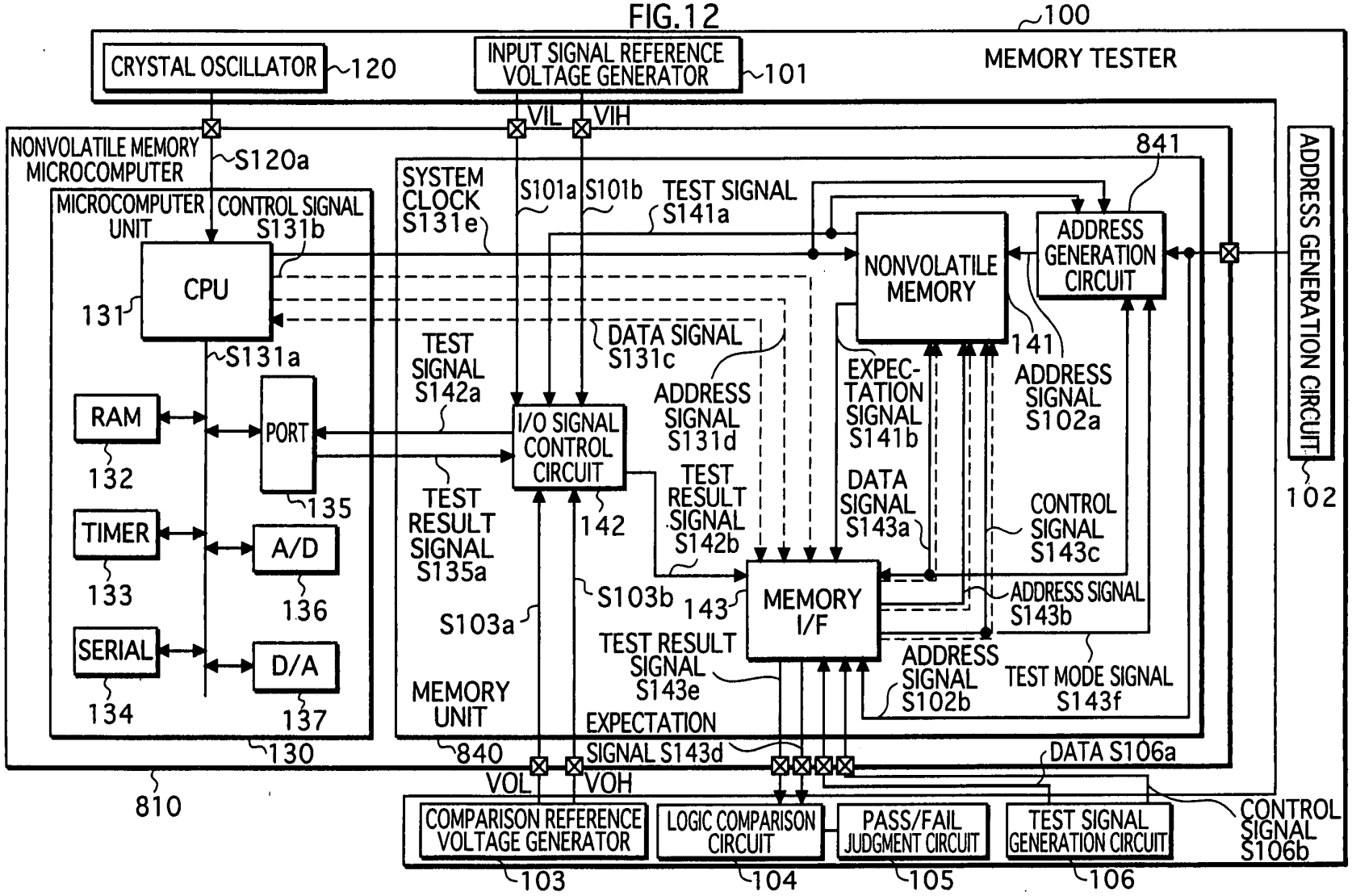

100
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
CPU
131
S131a
RAM
132
PORT
135
TIMER
133
A/D
136
SERIAL
134
D/A
137
130
810
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
841
NONVOLATILE MEMORY
ADDRESS GENERATION CIRCUIT
ADDRESS GENERATION CIRCUIT
102
141
TEST SIGNAL S142a
DATA SIGNAL S131c
ADDRESS SIGNAL S131d
EXPEC-TATION SIGNAL S141b
ADDRESS SIGNAL S102a
I/O SIGNAL CONTROL CIRCUIT
142
TEST RESULT SIGNAL S135a
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
S103a
S103b
143
MEMORY I/F
ADDRESS SIGNAL S143b
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL S102b
TEST MODE SIGNAL S143f
MEMORY UNIT
840
EXPECTATION SIGNAL S143d
DATA S106a
VOL
VOH
CONTROL SIGNAL S106b
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
103
104
105
106

FIG.13

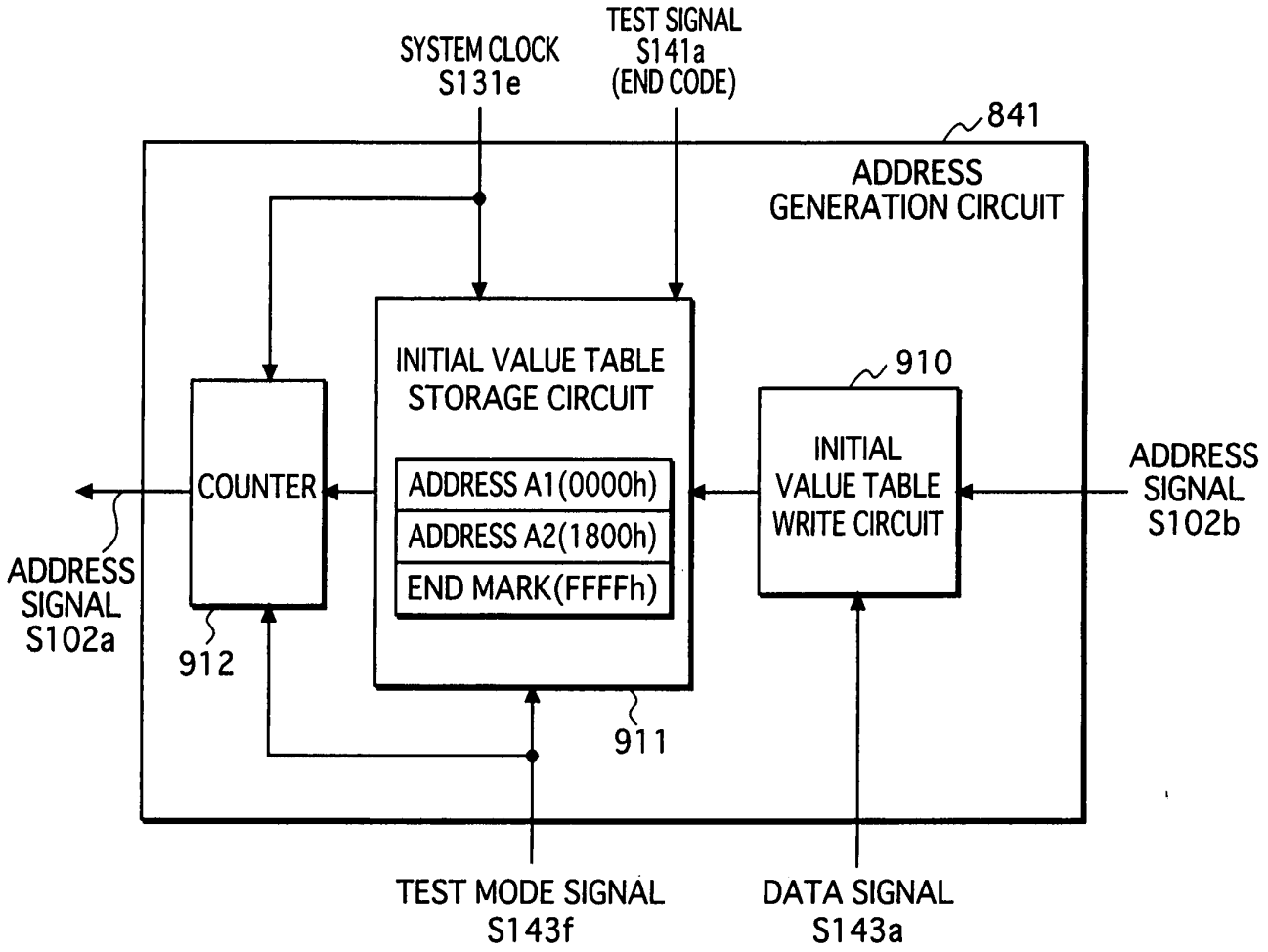

SYSTEM CLOCK
S131e
TEST SIGNAL
S141a
(END CODE)
841
ADDRESS
GENERATION CIRCUIT
INITIAL VALUE TABLE
STORAGE CIRCUIT
910
COUNTER
ADDRESS A1(0000h)
ADDRESS A2(1800h)
END MARK(FFFFh)
INITIAL
VALUE TABLE
WRITE CIRCUIT
ADDRESS
SIGNAL
S102b
ADDRESS
SIGNAL
S102a
912
911
TEST MODE SIGNAL
S143f
DATA SIGNAL
S143a

FIG.14

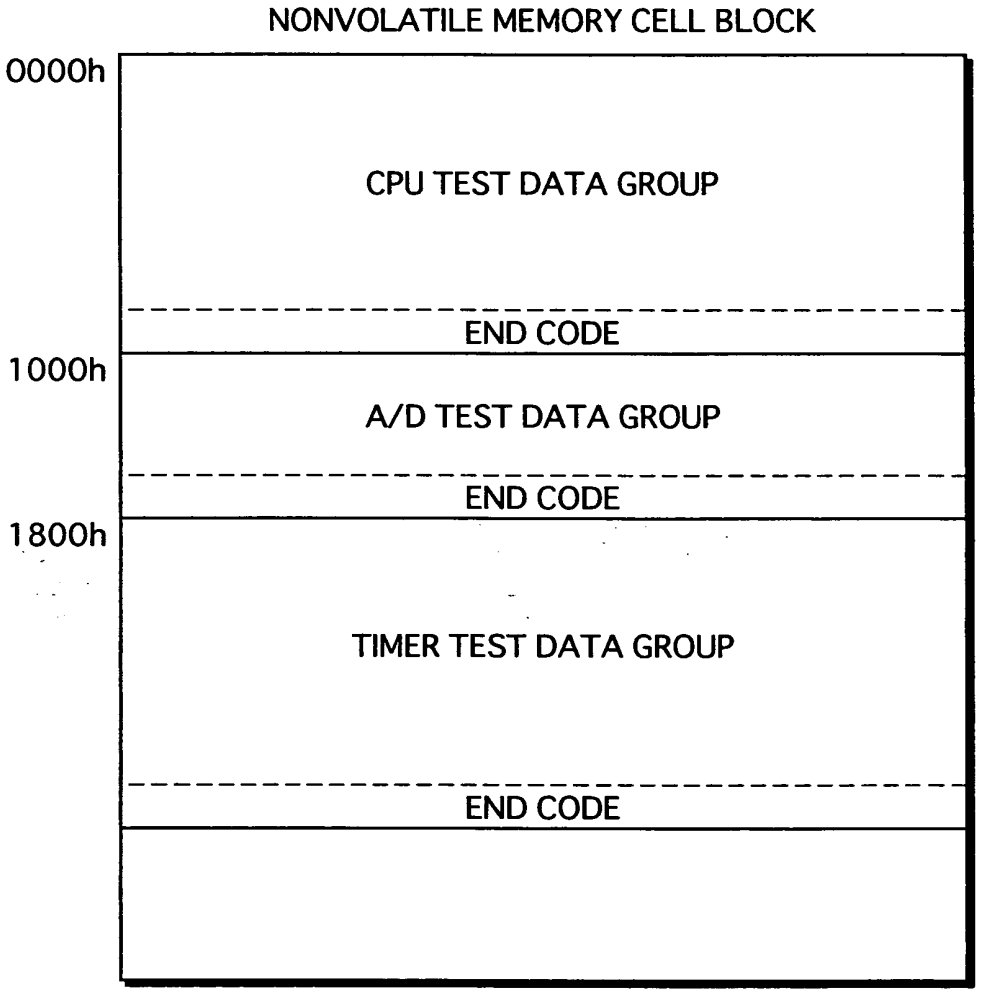

NONVOLATILE MEMORY CELL BLOCK
0000h
CPU TEST DATA GROUP
END CODE
1000h
A/D TEST DATA GROUP
END CODE
1800h
TIMER TEST DATA GROUP
END CODE

FIG.15

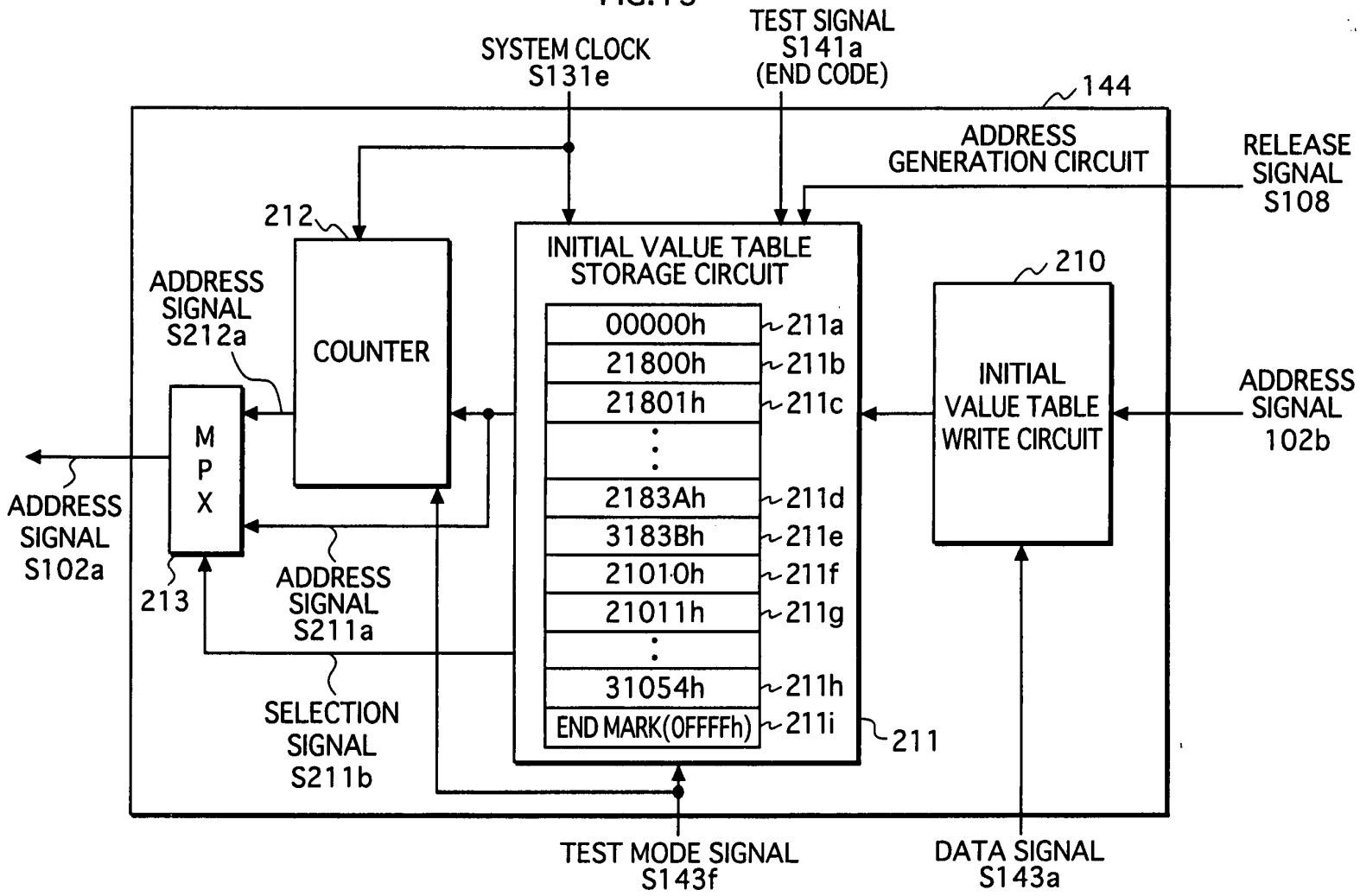

SYSTEM CLOCK
S131e
TEST SIGNAL
S141a
(END CODE)
144
ADDRESS
GENERATION CIRCUIT
RELEASE
SIGNAL
S108
212
COUNTER
INITIAL VALUE TABLE
STORAGE CIRCUIT
210
ADDRESS
SIGNAL
S212a
00000h
21800h
21801h
2183Ah
3183Bh
2101·0h
21011h
31054h
END MARK(0FFFFh)
211a
211b
211c
211d
211e
211f
211g
211h
211i
211
INITIAL
VALUE TABLE
WRITE CIRCUIT
ADDRESS
SIGNAL
102b
M
P
X
ADDRESS
SIGNAL
S102a
213
ADDRESS
SIGNAL
S211a
SELECTION
SIGNAL
S211b
TEST MODE SIGNAL
S143f
DATA SIGNAL
S143a

FIG.16

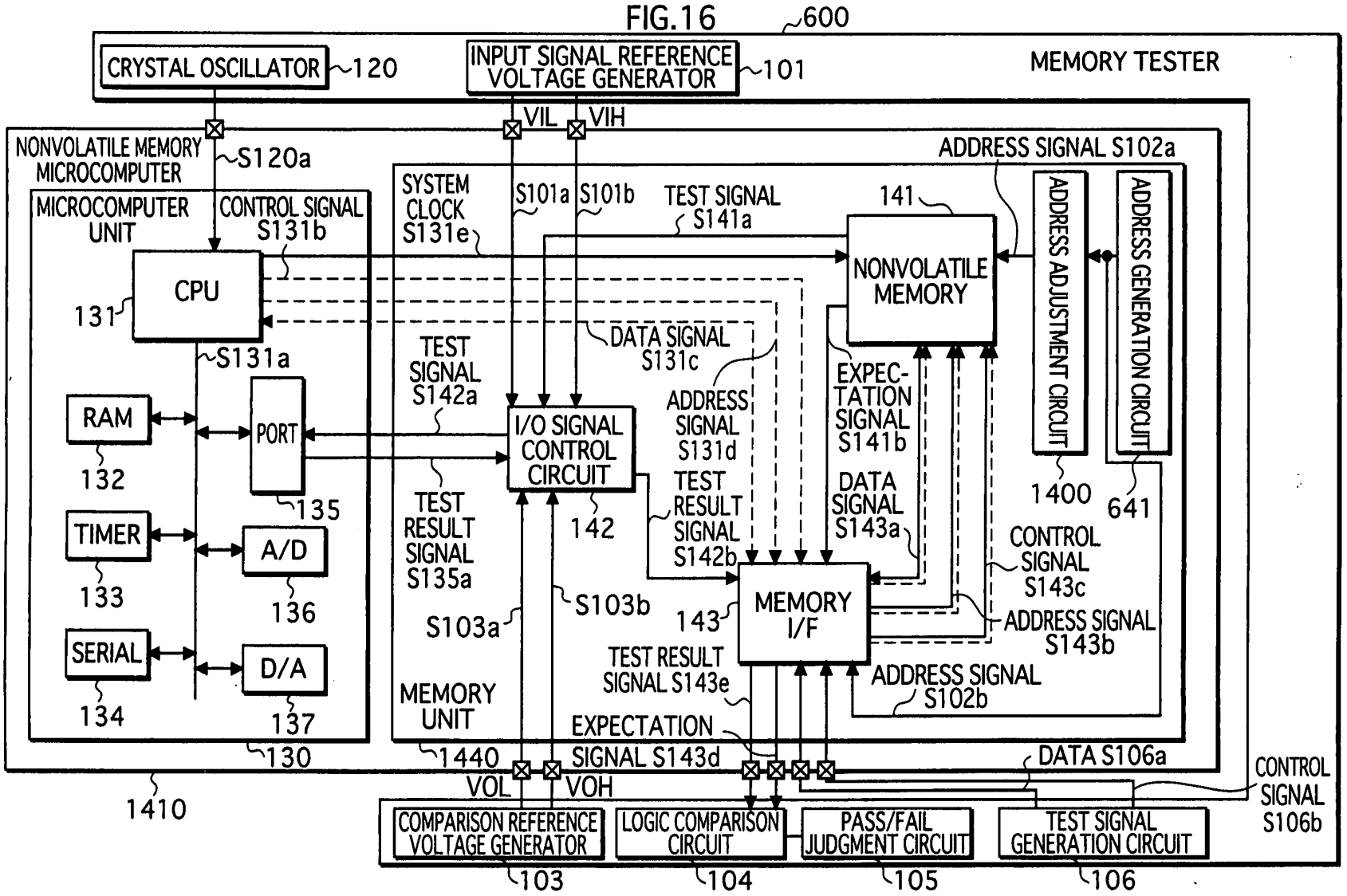

600
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
CPU
131
S131a
RAM
132
TIMER
133
SERIAL
134
PORT
135
A/D
136
D/A
137
130
1410
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
141
NONVOLATILE MEMORY
ADDRESS SIGNAL S102a
ADDRESS ADJUSTMENT CIRCUIT
ADDRESS GENERATION CIRCUIT
1400
641
DATA SIGNAL S131c
TEST SIGNAL S142a
ADDRESS SIGNAL S131d
EXPECTATION SIGNAL S141b
I/O SIGNAL CONTROL CIRCUIT
142
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
TEST RESULT SIGNAL S135a
S103a
S103b
143
MEMORY I/F
CONTROL SIGNAL S143c
ADDRESS SIGNAL S143b
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL S102b
MEMORY UNIT
EXPECTATION SIGNAL S143d
1440
VOL
VOH
DATA S106a
CONTROL SIGNAL S106b
COMPARISON REFERENCE VOLTAGE GENERATOR
103
LOGIC COMPARISON CIRCUIT
104
PASS/FAIL JUDGMENT CIRCUIT
105
TEST SIGNAL GENERATION CIRCUIT
106

FIG.17

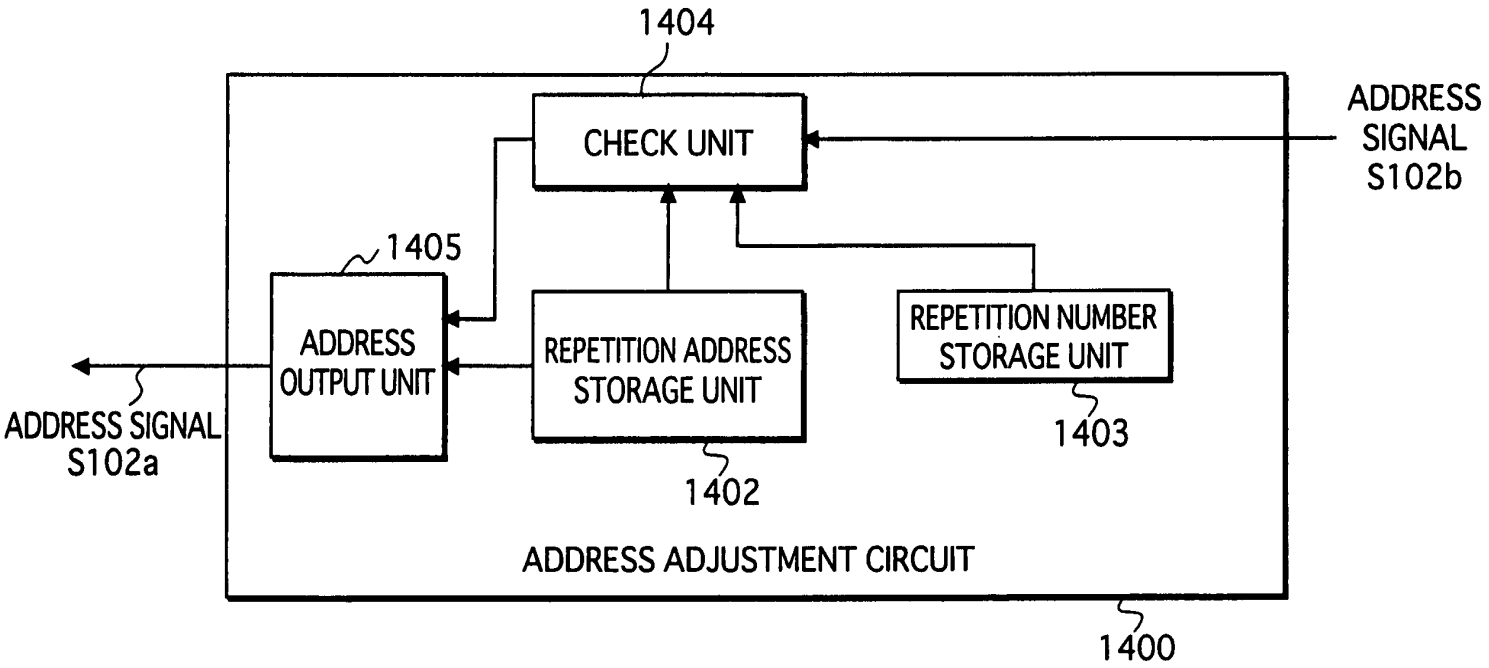

1404
CHECK UNIT
ADDRESS SIGNAL S102b
1405
ADDRESS OUTPUT UNIT
REPETITION ADDRESS STORAGE UNIT
REPETITION NUMBER STORAGE UNIT
ADDRESS SIGNAL S102a
1403
1402
ADDRESS ADJUSTMENT CIRCUIT
1400

FIG.18

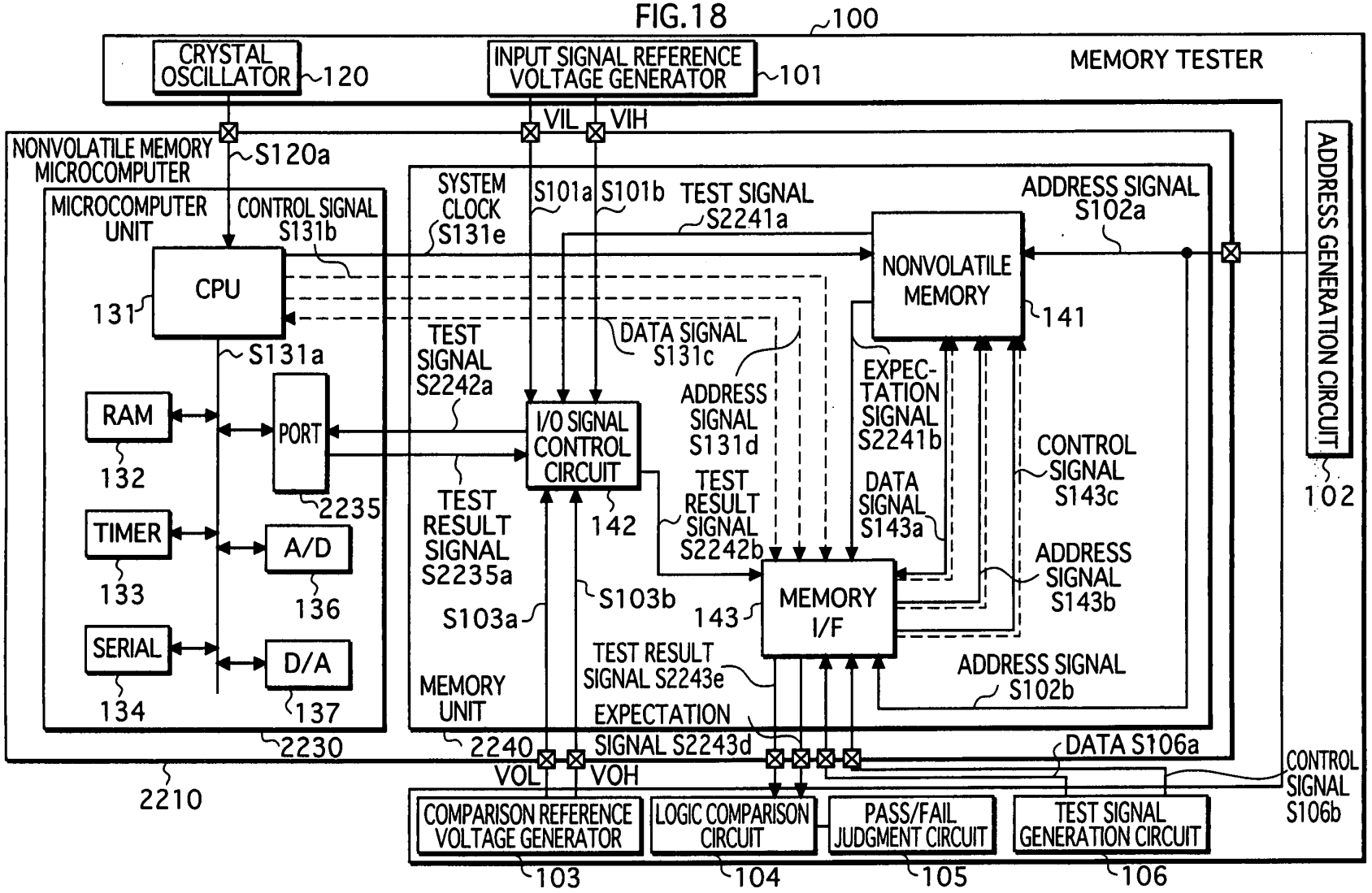

100
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S2241a
ADDRESS SIGNAL S102a
ADDRESS GENERATION CIRCUIT
102
CPU
131
NONVOLATILE MEMORY
141
S131a
TEST SIGNAL S2242a
DATA SIGNAL S131c
EXPEC-TATION SIGNAL S2241b
ADDRESS SIGNAL S131d
RAM
132
PORT
2235
I/O SIGNAL CONTROL CIRCUIT
142
CONTROL SIGNAL S143c
TIMER
133
A/D
136
TEST RESULT SIGNAL S2235a
TEST RESULT SIGNAL S2242b
DATA SIGNAL S143a
ADDRESS SIGNAL S143b
S103a
S103b
143
MEMORY I/F
SERIAL
134
D/A
137
TEST RESULT SIGNAL S2243e
ADDRESS SIGNAL S102b
MEMORY UNIT
2240
EXPECTATION SIGNAL S2243d
DATA S106a
2230
VOL
VOH
CONTROL SIGNAL S106b
2210
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
103
104
105
106

FIG.19

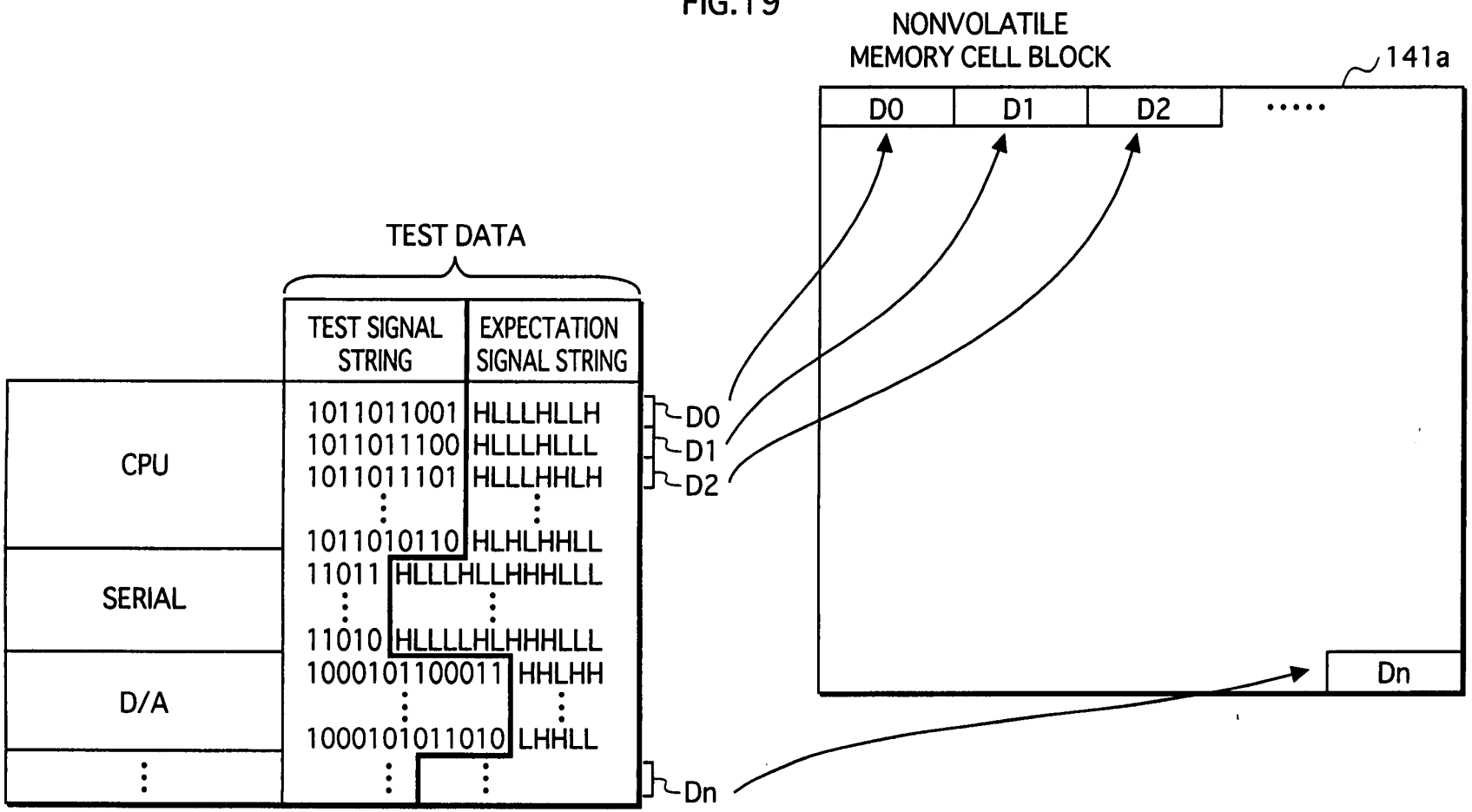

NONVOLATILE
MEMORY CELL BLOCK
141a
D0
D1
D2
.....
Dn
TEST DATA
TEST SIGNAL STRING
EXPECTATION SIGNAL STRING
CPU
SERIAL
D/A
1011011001 HLLLHLLH
1011011100 HLLLHLLL
1011011101 HLLLHHLH
1011010110 HLHLHHLL
11011 HLLLHLLHHHLLL
11010 HLLLLHLHHHLLL
1000101100011 HHLHH
1000101011010 LHHLL
D0
D1
D2
Dn

FIG.20

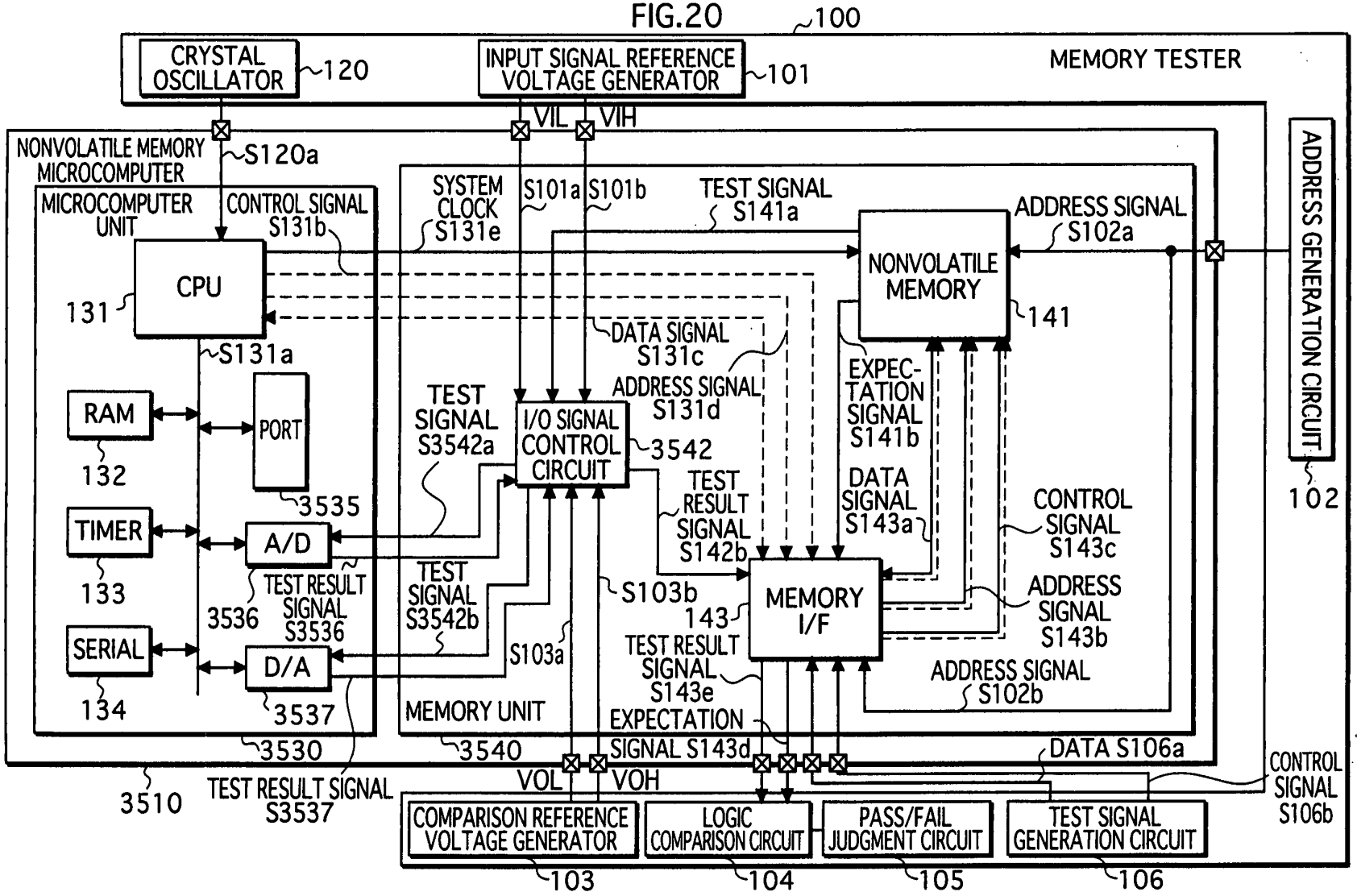

100
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
ADDRESS SIGNAL S102a
ADDRESS GENERATION CIRCUIT
102
CPU
131
S131a
NONVOLATILE MEMORY
141
DATA SIGNAL S131c
EXPEC-TATION SIGNAL S141b
RAM
132
PORT
3535
TEST SIGNAL S3542a
I/O SIGNAL CONTROL CIRCUIT
3542
ADDRESS SIGNAL S131d
TIMER
133
A/D
3536
TEST RESULT SIGNAL S3536
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
SERIAL
134
D/A
3537
TEST SIGNAL S3542b
S103a
S103b
MEMORY I/F
143
ADDRESS SIGNAL S143b
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL S102b
MEMORY UNIT
EXPECTATION SIGNAL S143d
3530
3540
DATA S106a
CONTROL SIGNAL S106b
VOL
VOH
3510
TEST RESULT SIGNAL S3537
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
103
104
105
106

FIG. 21

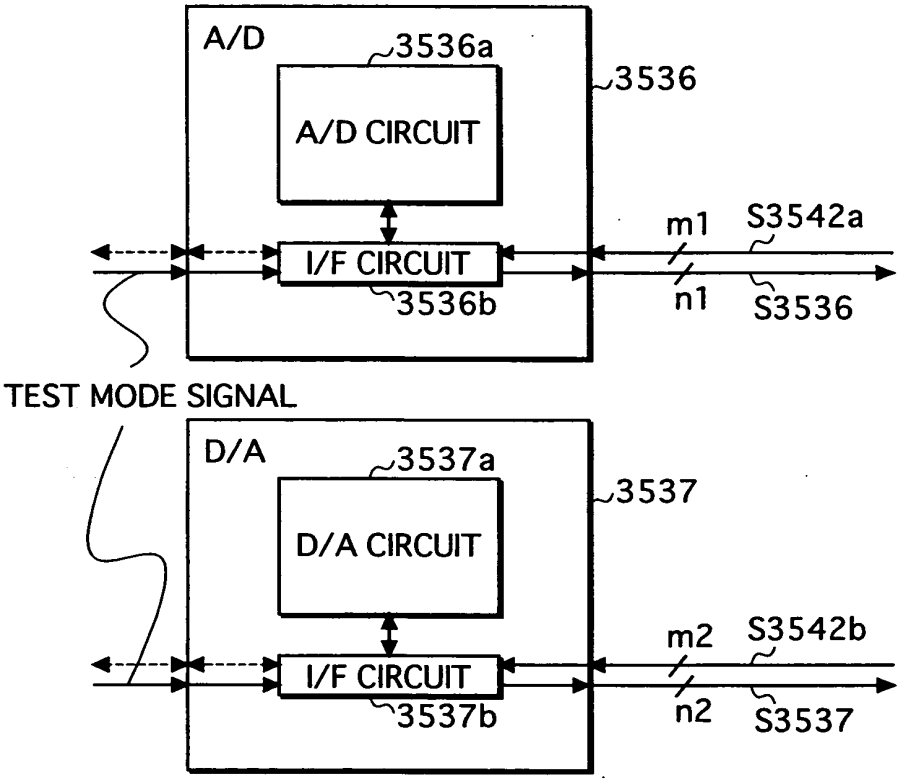

A/D
3536a
3536
A/D CIRCUIT
m1
S3542a
I/F CIRCUIT
3536b
n1
S3536
TEST MODE SIGNAL
D/A
3537a
3537
D/A CIRCUIT
m2
S3542b
I/F CIRCUIT
3537b
n2
S3537

FIG.22

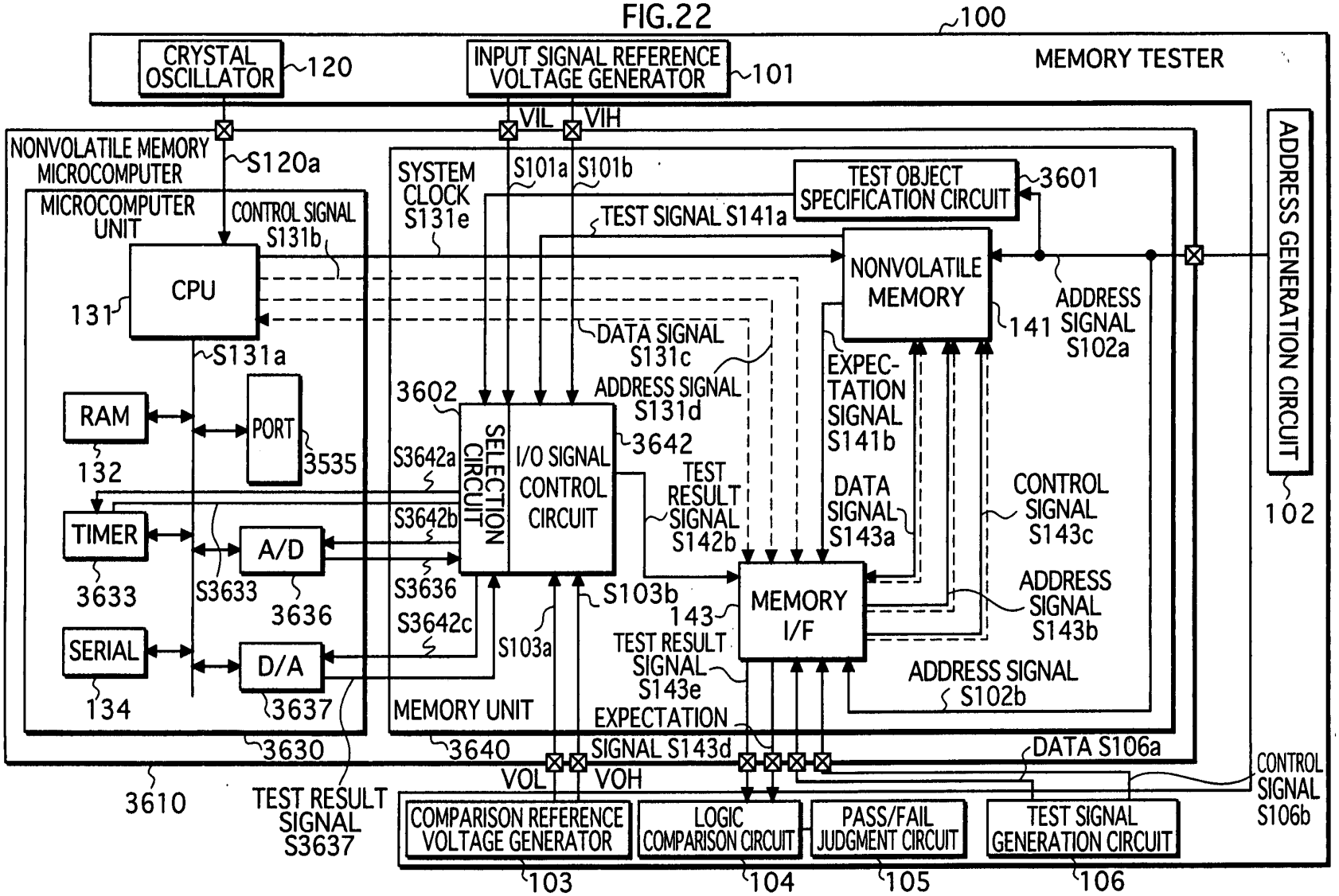

100
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
SYSTEM CLOCK S131e
S101a
S101b
TEST OBJECT SPECIFICATION CIRCUIT
3601
TEST SIGNAL S141a
CPU
131
S131a
NONVOLATILE MEMORY
141
ADDRESS SIGNAL S102a
DATA SIGNAL S131c
EXPEC-TATION SIGNAL S141b
ADDRESS SIGNAL S131d
3602
RAM
132
PORT
3535
SELECTION CIRCUIT
I/O SIGNAL CONTROL CIRCUIT
3642
S3642a
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
TIMER
3633
S3642b
A/D
3636
S3633
S3636
S103b
143
MEMORY I/F
ADDRESS SIGNAL S143b
SERIAL
134
S3642c
S103a
D/A
3637
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL S102b
MEMORY UNIT
EXPECTATION SIGNAL S143d
DATA S106a
3630
3640
VOL
VOH
3610
TEST RESULT SIGNAL S3637
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
ADDRESS GENERATION CIRCUIT
102
CONTROL SIGNAL S106b
103
104
105
106

FIG. 23

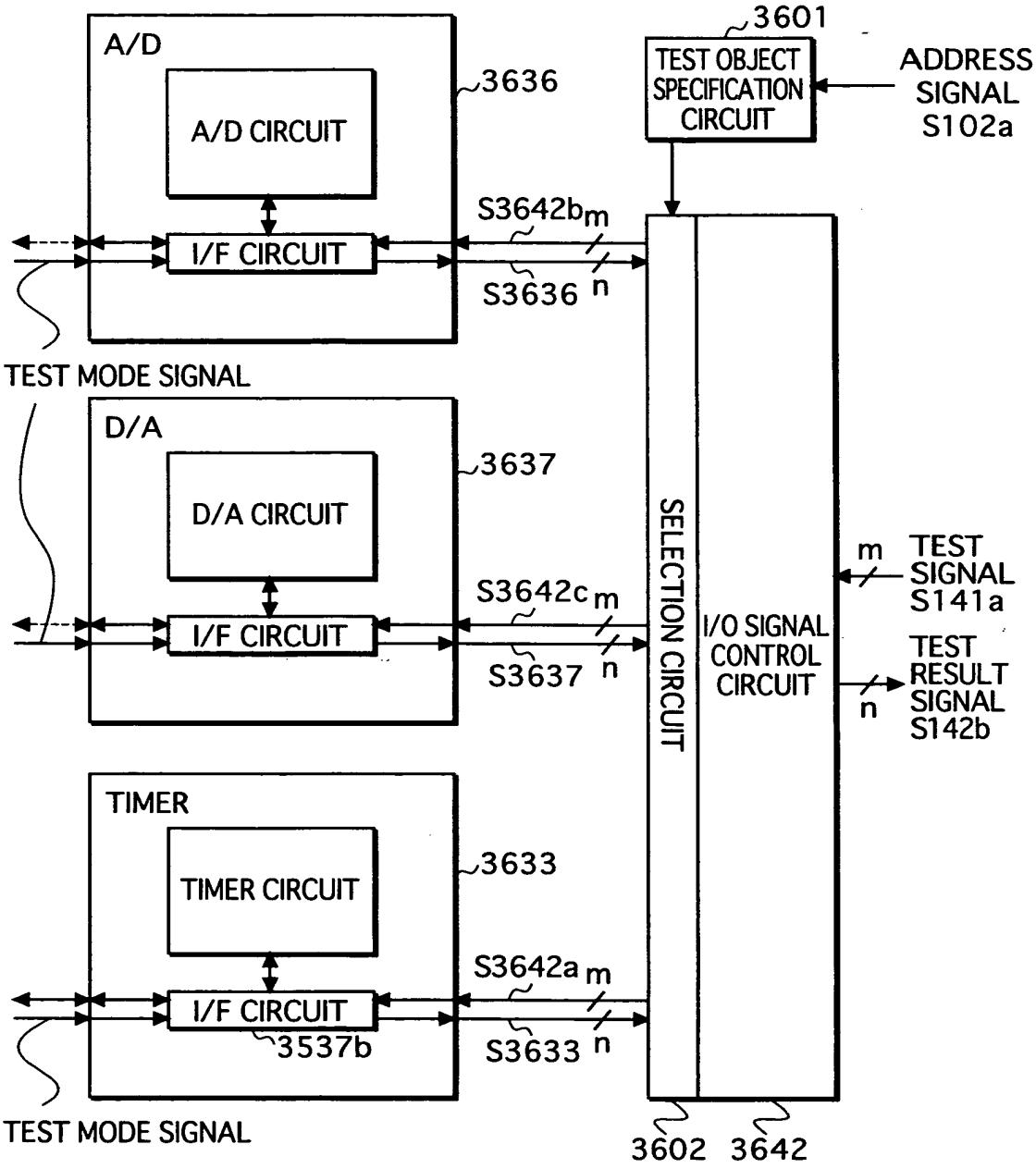

A/D
A/D CIRCUIT
I/F CIRCUIT
3636
S3642b m
S3636 n
TEST MODE SIGNAL
D/A
D/A CIRCUIT
I/F CIRCUIT
3637
S3642c m
S3637 n
TIMER
TIMER CIRCUIT
I/F CIRCUIT
3537b
3633
S3642a m
S3633 n
TEST MODE SIGNAL
3601
TEST OBJECT SPECIFICATION CIRCUIT
ADDRESS SIGNAL S102a
SELECTION CIRCUIT
I/O SIGNAL CONTROL CIRCUIT
m TEST SIGNAL S141a
n TEST RESULT SIGNAL S142b
3602
3642

FIG.24

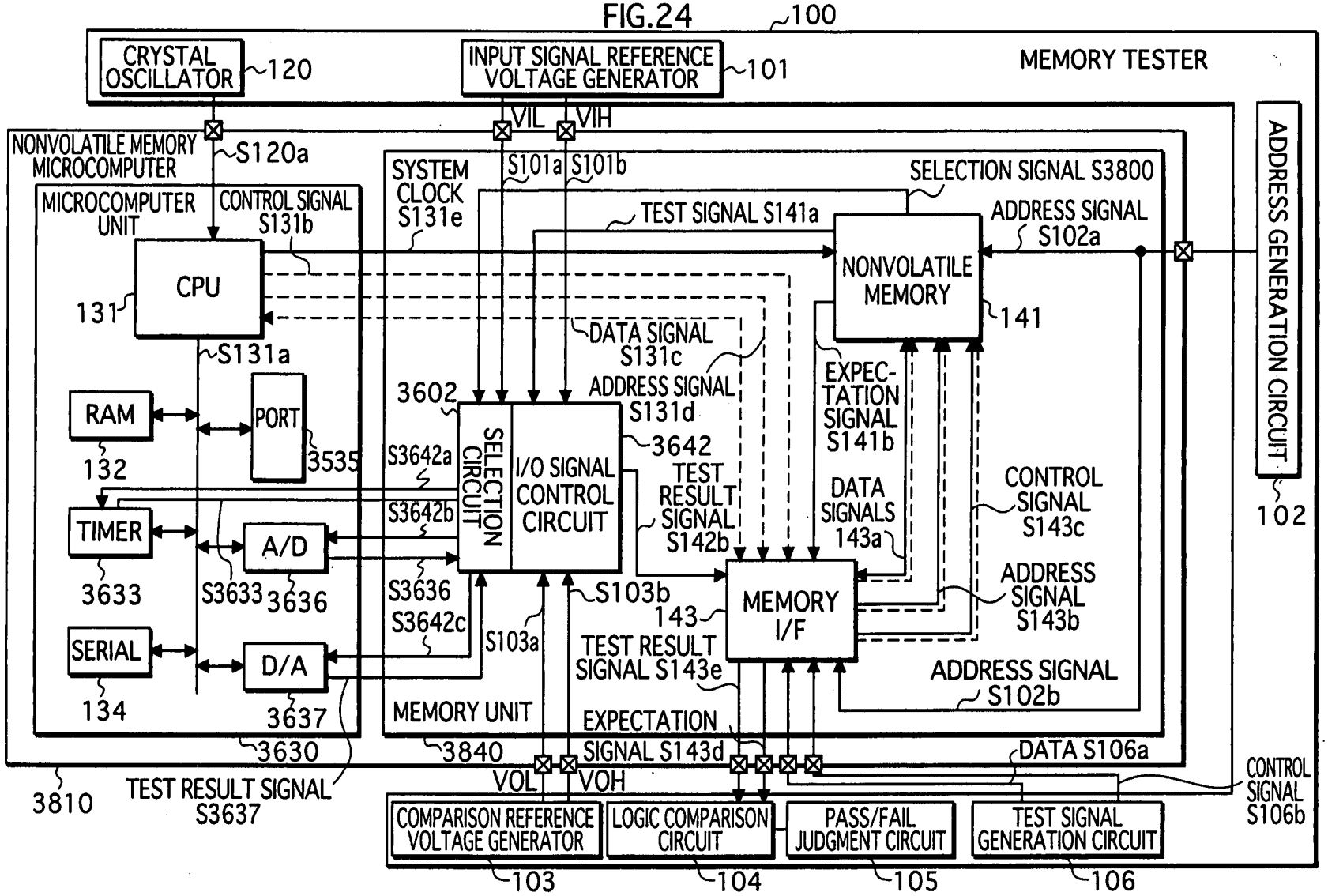

100
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
ADDRESS GENERATION CIRCUIT
102
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
CPU
131
S131a
RAM
132
PORT
3535
TIMER
3633
S3633
A/D
3636
SERIAL
134
D/A
3637
3630
3810
TEST RESULT SIGNAL S3637
SYSTEM CLOCK S131e
S101a
S101b
SELECTION SIGNAL S3800
TEST SIGNAL S141a
ADDRESS SIGNAL S102a
NONVOLATILE MEMORY
141
DATA SIGNAL S131c
ADDRESS SIGNAL S131d
EXPEC-TATION SIGNAL S141b
3602
SELECTION CIRCUIT
I/O SIGNAL CONTROL CIRCUIT
3642
S3642a
S3642b
S3642c
S3636
TEST RESULT SIGNAL S142b
DATA SIGNALS 143a
CONTROL SIGNAL S143c
ADDRESS SIGNAL S143b
S103b
143
MEMORY I/F
S103a
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL S102b
MEMORY UNIT
3840
EXPECTATION SIGNAL S143d
DATA S106a
CONTROL SIGNAL S106b
VOL
VOH
COMPARISON REFERENCE VOLTAGE GENERATOR
103
LOGIC COMPARISON CIRCUIT
104
PASS/FAIL JUDGMENT CIRCUIT
105
TEST SIGNAL GENERATION CIRCUIT
106

FIG.25

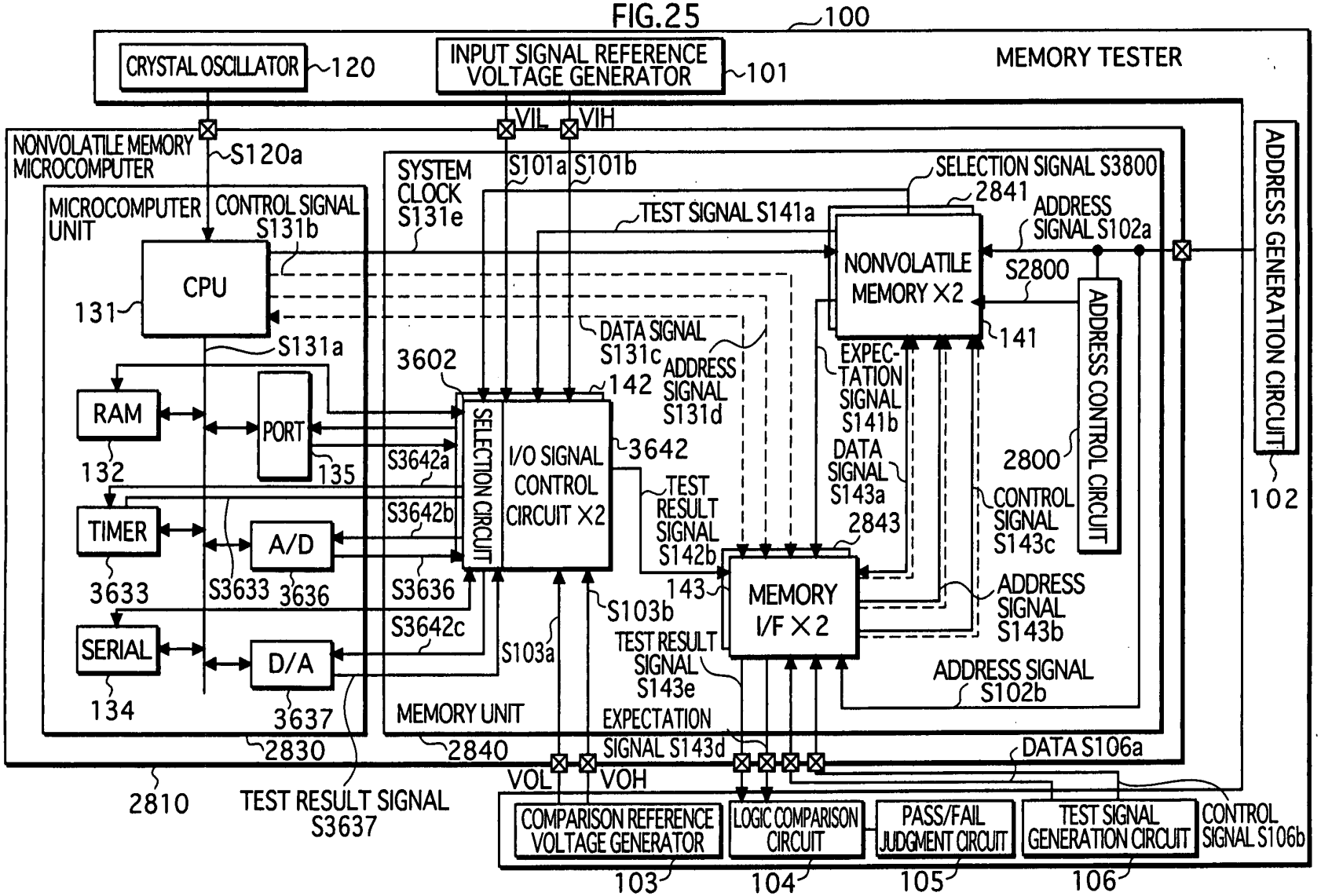

100
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
CPU
131
S131a
RAM
132
PORT
135
TIMER
3633
A/D
3636
SERIAL
134
D/A
3637
S3633
2830
2810
TEST RESULT SIGNAL S3637
SYSTEM CLOCK S131e
S101a
S101b
3602
SELECTION CIRCUIT
I/O SIGNAL CONTROL CIRCUIT X2
3642
S3642a
S3642b
S3636
S3642c
S103a
S103b
142
DATA SIGNAL S131c
ADDRESS SIGNAL S131d
TEST RESULT SIGNAL S142b
143
TEST RESULT SIGNAL S143e
MEMORY UNIT
2840
EXPECTATION SIGNAL S143d
VOL
VOH
SELECTION SIGNAL S3800
2841
TEST SIGNAL S141a
NONVOLATILE MEMORY X2
141
S2800
ADDRESS SIGNAL S102a
EXPEC-TATION SIGNAL S141b
DATA SIGNAL S143a
2843
MEMORY I/F X2
ADDRESS SIGNAL S143b
ADDRESS SIGNAL S102b
ADDRESS CONTROL CIRCUIT
2800
CONTROL SIGNAL S143c
ADDRESS GENERATION CIRCUIT
102
DATA S106a
CONTROL SIGNAL S106b
COMPARISON REFERENCE VOLTAGE GENERATOR
103
LOGIC COMPARISON CIRCUIT
104
PASS/FAIL JUDGMENT CIRCUIT
105
TEST SIGNAL GENERATION CIRCUIT
106

FIG. 26

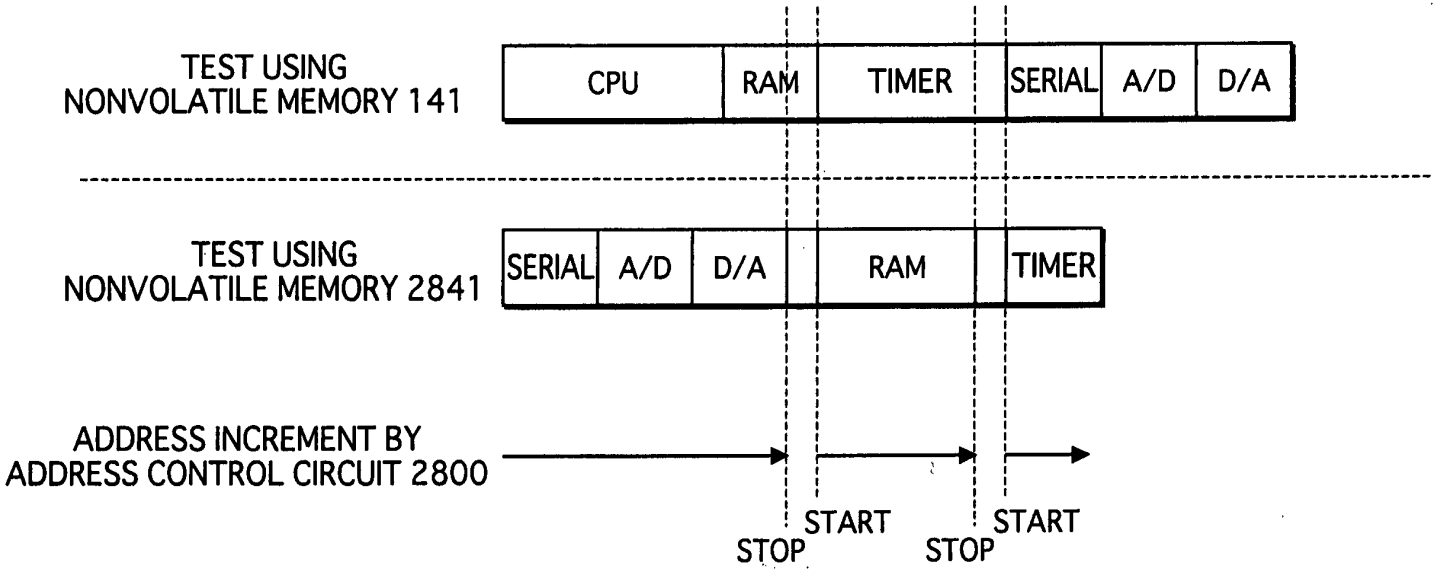

TEST USING
NONVOLATILE MEMORY 141
CPU
RAM
TIMER
SERIAL
A/D
D/A
TEST USING
NONVOLATILE MEMORY 2841
SERIAL
A/D
D/A
RAM
TIMER
ADDRESS INCREMENT BY
ADDRESS CONTROL CIRCUIT 2800
STOP
START
STOP
START

FIG.27

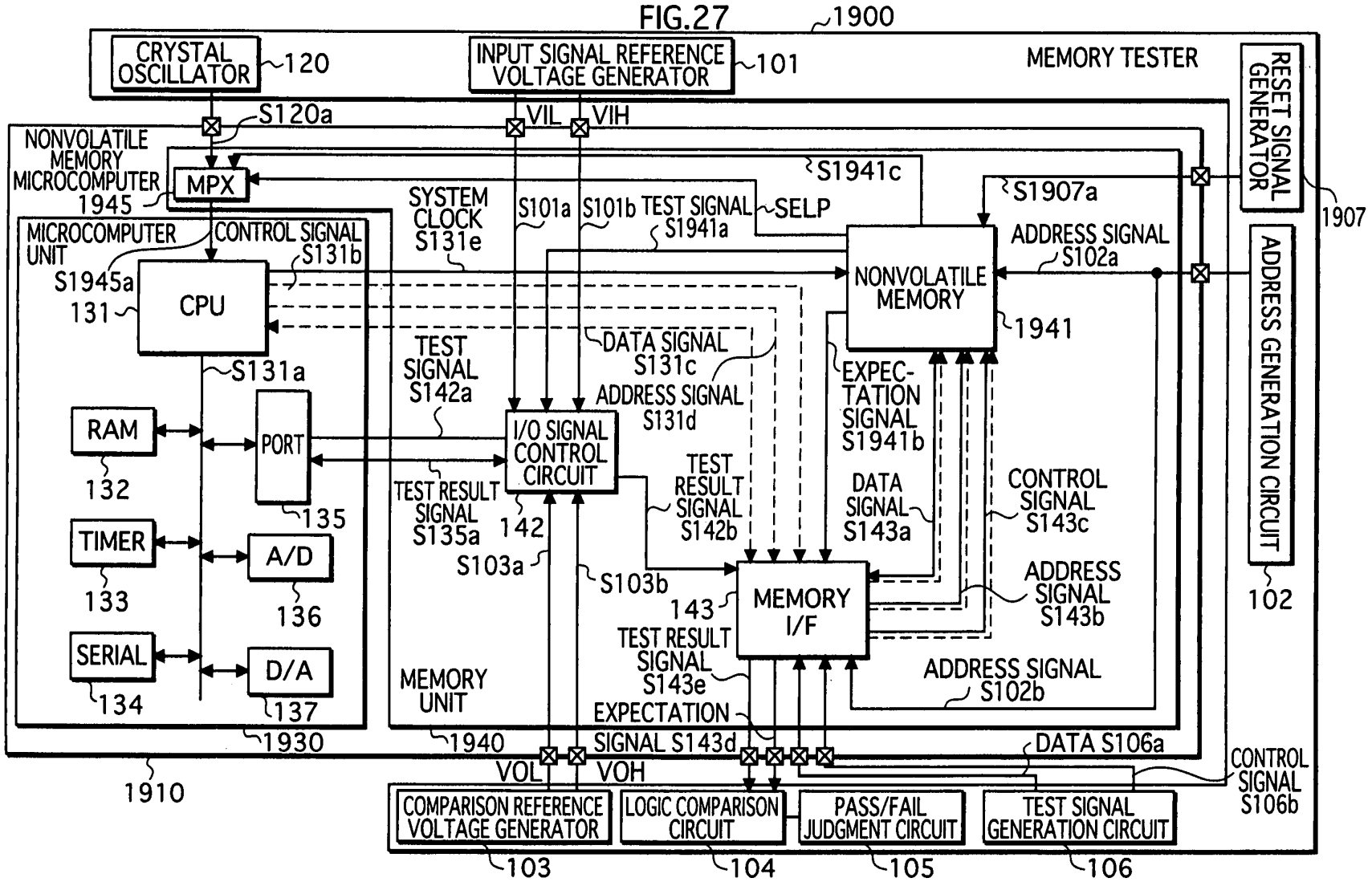

1900
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
MEMORY TESTER
RESET SIGNAL GENERATOR
1907
S120a
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
1945
MPX
S1941c
S1907a
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S1941a
SELP
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
S1945a
131
CPU
NONVOLATILE MEMORY
1941
ADDRESS SIGNAL S102a
ADDRESS GENERATION CIRCUIT
102
S131a
TEST SIGNAL S142a
DATA SIGNAL S131c
ADDRESS SIGNAL S131d
EXPEC-TATION SIGNAL S1941b
RAM
132
PORT
135
I/O SIGNAL CONTROL CIRCUIT
TEST RESULT SIGNAL S135a
142
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
TIMER
133
A/D
136
S103a
S103b
143
MEMORY I/F
ADDRESS SIGNAL S143b
SERIAL
134
D/A
137
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL S102b
MEMORY UNIT
EXPECTATION SIGNAL S143d
1930
1940
DATA S106a
CONTROL SIGNAL S106b
1910
VOL
VOH
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
103
104
105
106

FIG.28

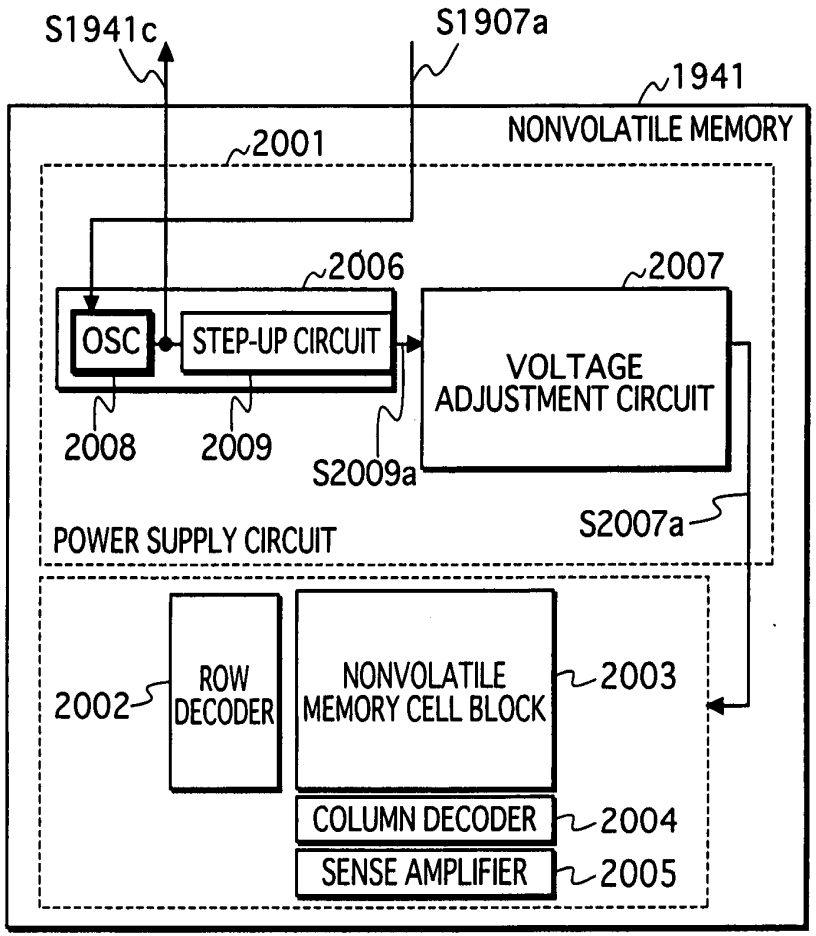

S1941c
S1907a
1941
NONVOLATILE MEMORY
2001
2006
2007
OSC
STEP-UP CIRCUIT
VOLTAGE ADJUSTMENT CIRCUIT
2008
2009
S2009a
S2007a
POWER SUPPLY CIRCUIT
2002
ROW DECODER
NONVOLATILE MEMORY CELL BLOCK
2003
COLUMN DECODER
2004
SENSE AMPLIFIER
2005

FIG.29

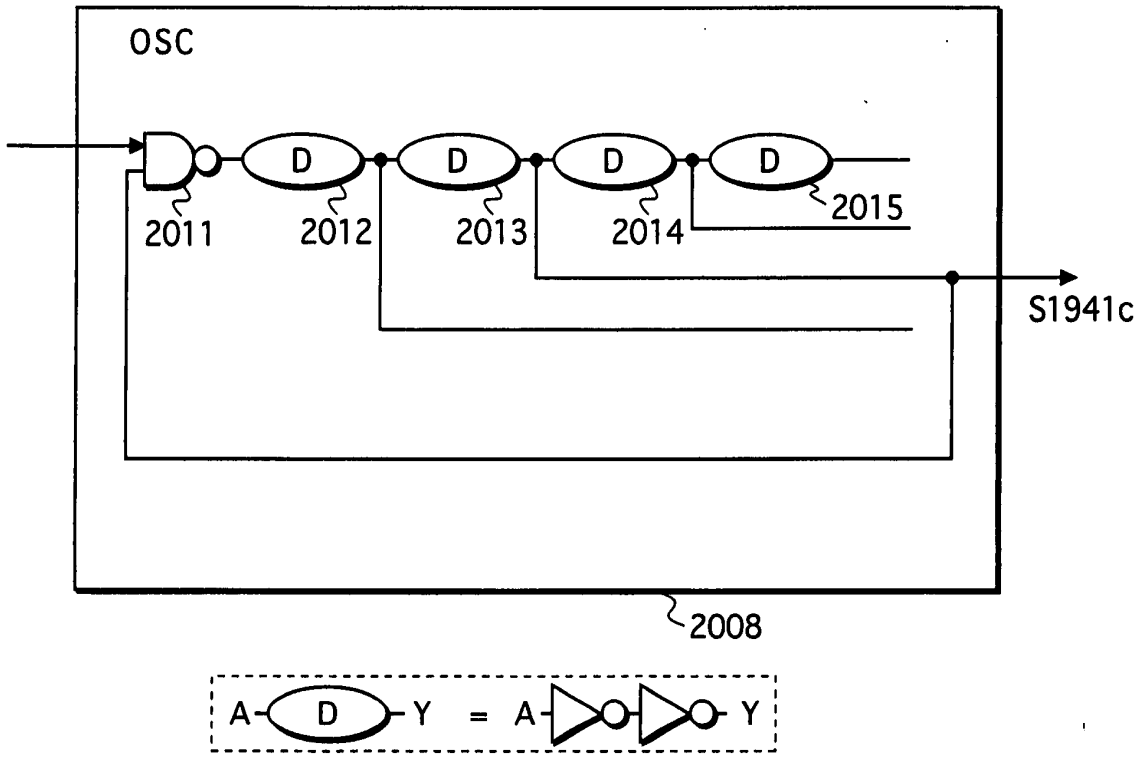


FIG.30

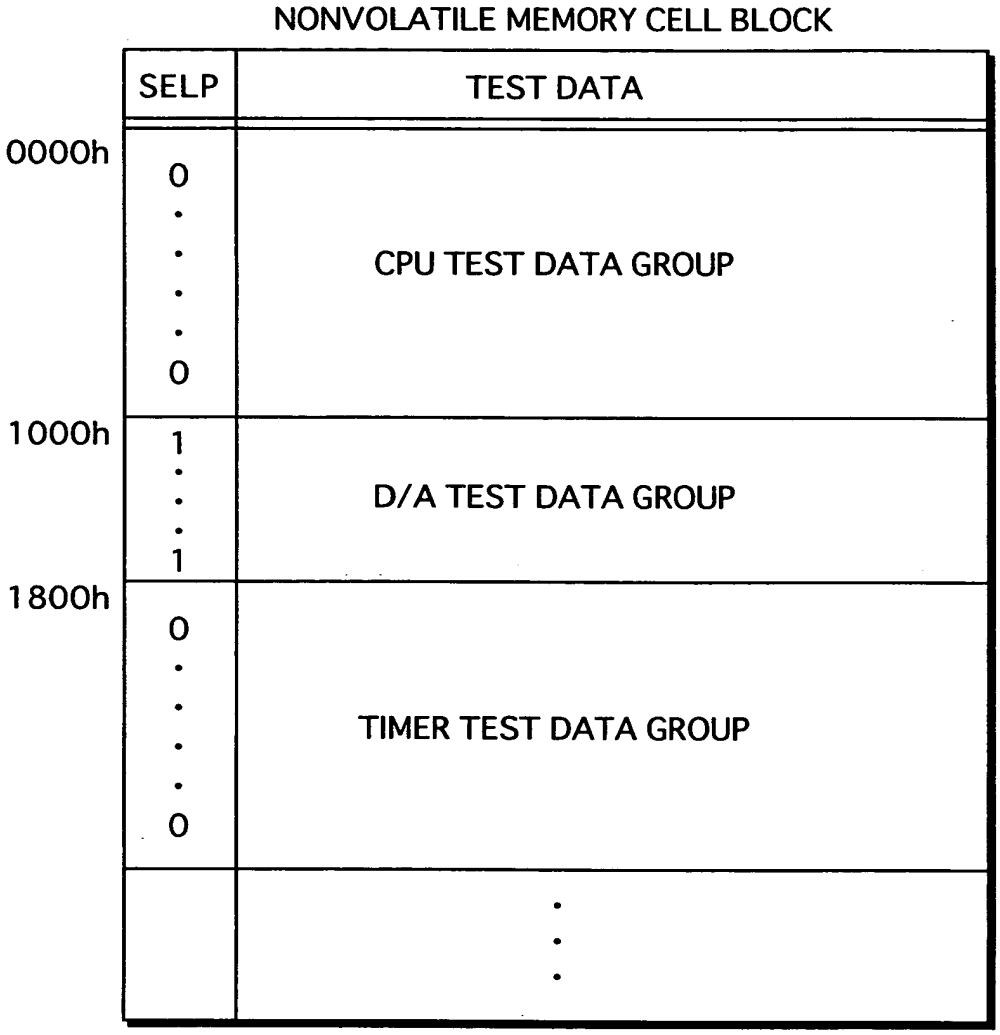

NONVOLATILE MEMORY CELL BLOCK
SELP
TEST DATA
0000h
0
0
CPU TEST DATA GROUP
1000h
1
1
D/A TEST DATA GROUP
1800h
0
0
TIMER TEST DATA GROUP

FIG. 31

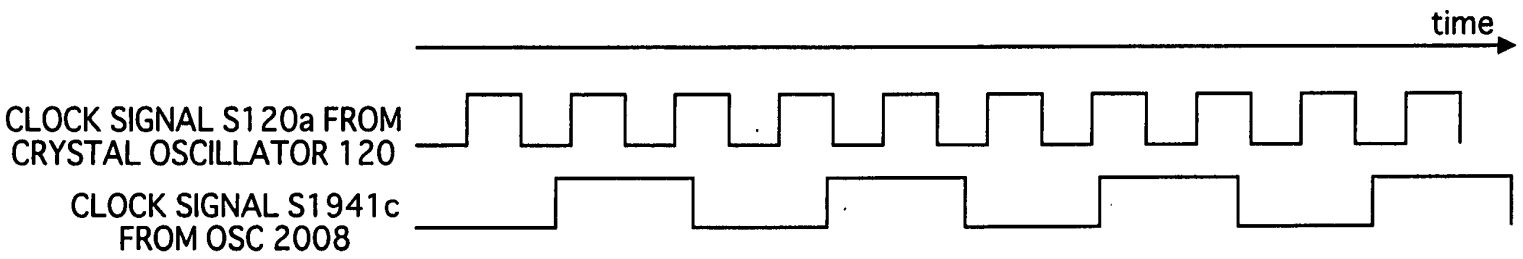

time
CLOCK SIGNAL S120a FROM CRYSTAL OSCILLATOR 120
CLOCK SIGNAL S1941c FROM OSC 2008

FIG.32

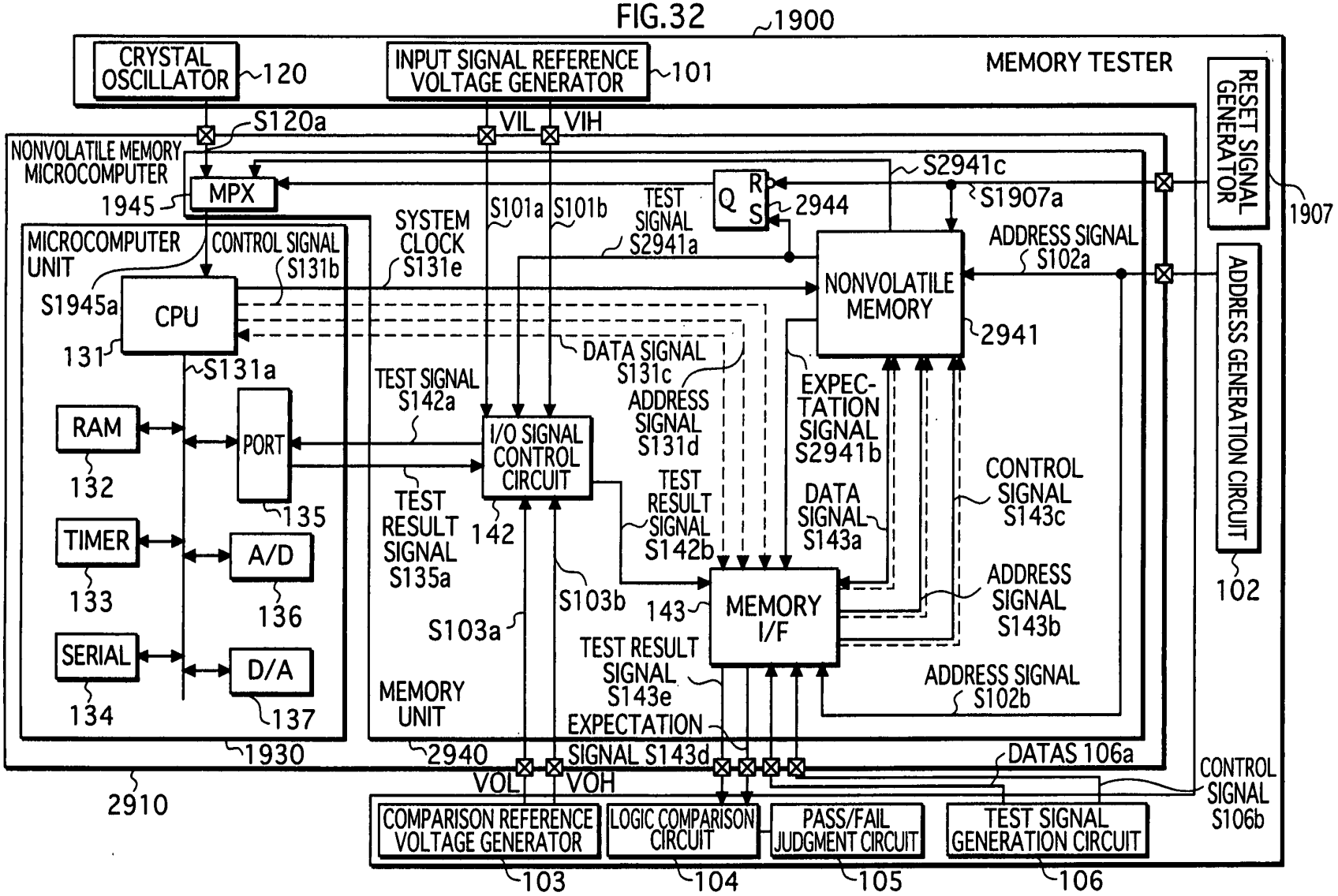

1900
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
RESET SIGNAL GENERATOR
1907
S120a
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
MPX
1945
S2941c
S1907a
Q
R
S
2944
TEST SIGNAL S2941a
S101a
S101b
SYSTEM CLOCK S131e
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
S1945a
CPU
131
S131a
NONVOLATILE MEMORY
2941
ADDRESS SIGNAL S102a
ADDRESS GENERATION CIRCUIT
102
DATA SIGNAL S131c
TEST SIGNAL S142a
ADDRESS SIGNAL S131d
EXPEC-TATION SIGNAL S2941b
RAM
132
PORT
135
I/O SIGNAL CONTROL CIRCUIT
142
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
TIMER
133
A/D
136
TEST RESULT SIGNAL S135a
S103b
143
MEMORY I/F
ADDRESS SIGNAL S143b
S103a
SERIAL
134
D/A
137
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL S102b
MEMORY UNIT
EXPECTATION SIGNAL S143d
1930
2940
DATAS 106a
CONTROL SIGNAL S106b
2910
VOL
VOH
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
103
104
105
106

FIG. 33

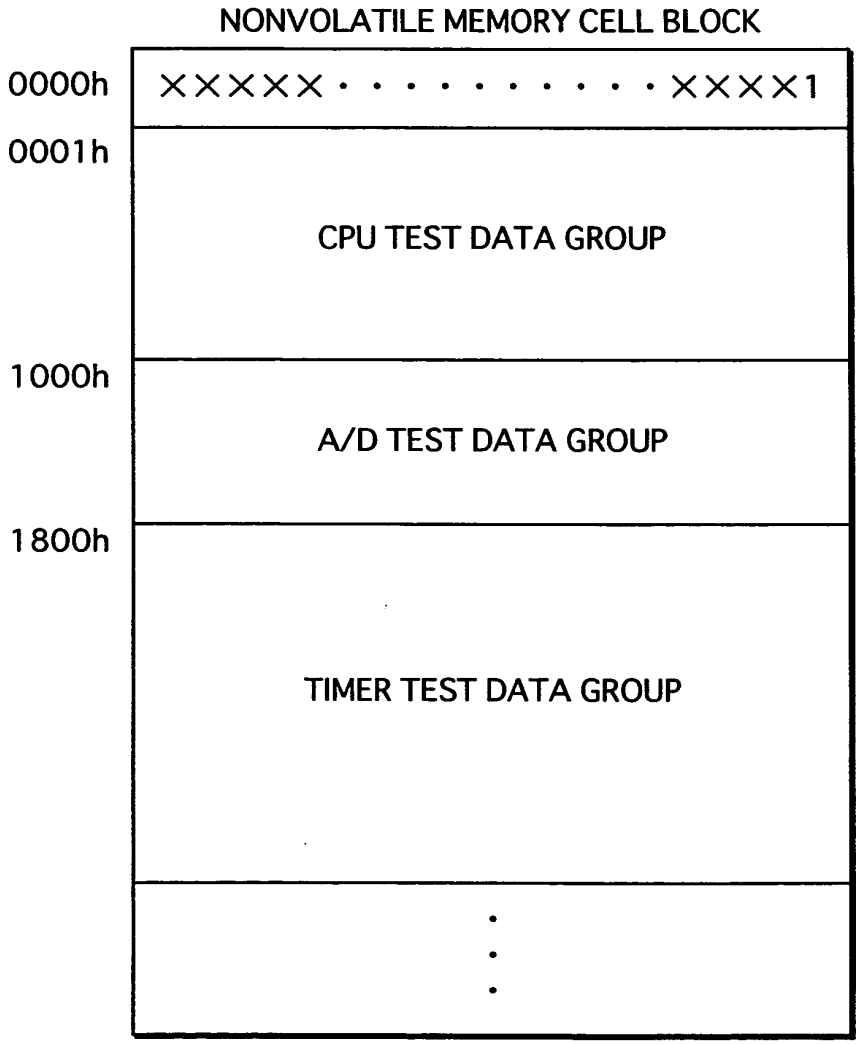

NONVOLATILE MEMORY CELL BLOCK
0000h
××××× · · · · · · · · · · ××××1
0001h
CPU TEST DATA GROUP
1000h
A/D TEST DATA GROUP
1800h
TIMER TEST DATA GROUP

FIG.34

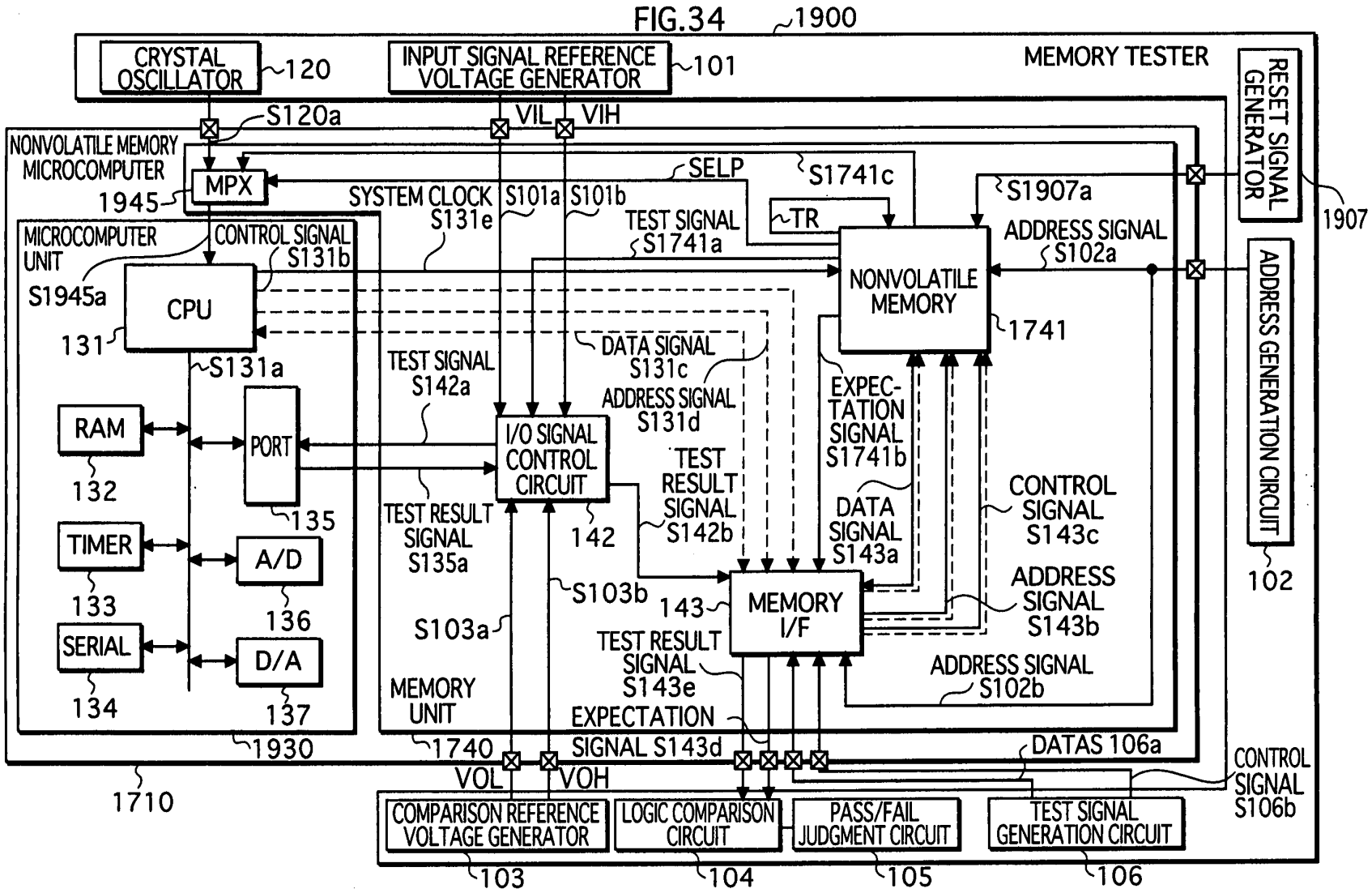

1900
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
MEMORY TESTER
RESET SIGNAL GENERATOR
1907
S120a
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
MPX
1945
SELP
S1741c
SYSTEM CLOCK
S131e
S101a
S101b
TEST SIGNAL
S1741a
TR
S1907a
ADDRESS SIGNAL
S102a
MICROCOMPUTER UNIT
CONTROL SIGNAL
S131b
S1945a
CPU
131
NONVOLATILE MEMORY
1741
ADDRESS GENERATION CIRCUIT
102
S131a
TEST SIGNAL
S142a
DATA SIGNAL
S131c
ADDRESS SIGNAL
S131d
EXPEC-TATION SIGNAL
S1741b
RAM
132
PORT
135
I/O SIGNAL CONTROL CIRCUIT
142
TEST RESULT SIGNAL
S142b
CONTROL SIGNAL
S143c
TEST RESULT SIGNAL
S135a
DATA SIGNAL
S143a
TIMER
133
A/D
136
S103b
143
MEMORY I/F
ADDRESS SIGNAL
S143b
S103a
SERIAL
134
D/A
137
TEST RESULT SIGNAL
S143e
ADDRESS SIGNAL
S102b
MEMORY UNIT
EXPECTATION
1930
1740
SIGNAL S143d
DATAS 106a
CONTROL SIGNAL
S106b
1710
VOL
VOH
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
103
104
105
106

FIG.35

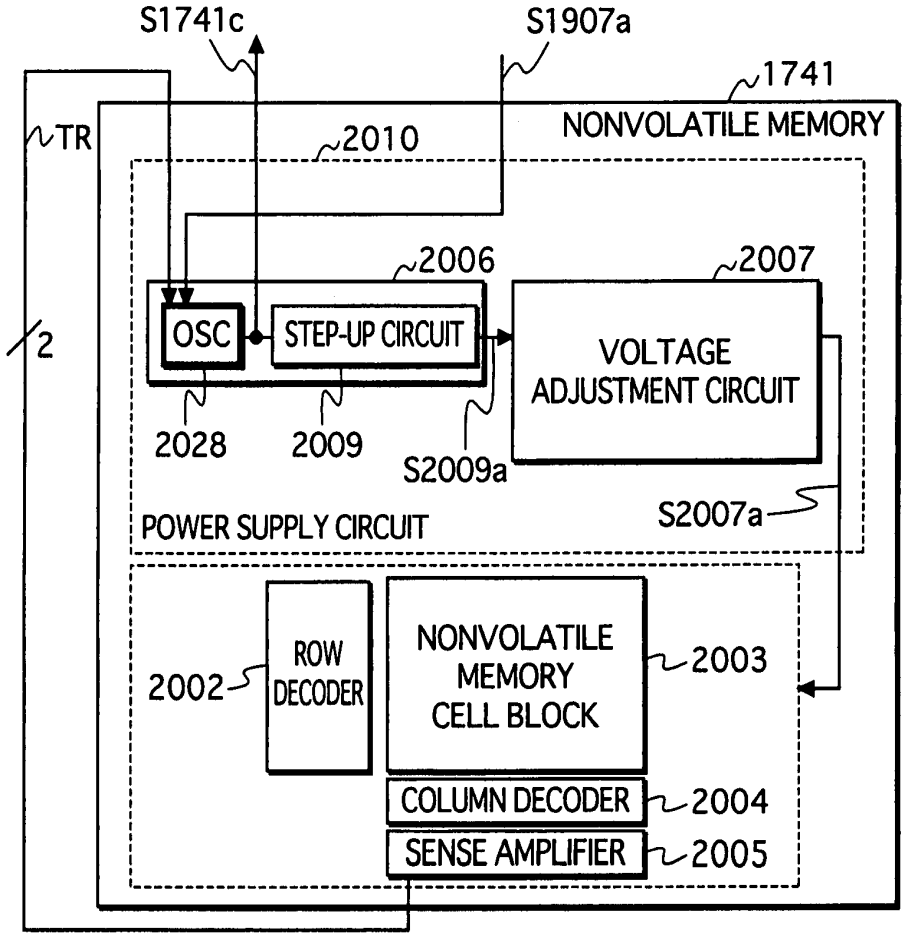

S1741c
S1907a
1741
NONVOLATILE MEMORY
TR
2010
2006
2007
OSC
STEP-UP CIRCUIT
VOLTAGE ADJUSTMENT CIRCUIT
2
2028
2009
S2009a
POWER SUPPLY CIRCUIT
S2007a
2002
ROW DECODER
NONVOLATILE MEMORY CELL BLOCK
2003
COLUMN DECODER
2004
SENSE AMPLIFIER
2005

FIG.36

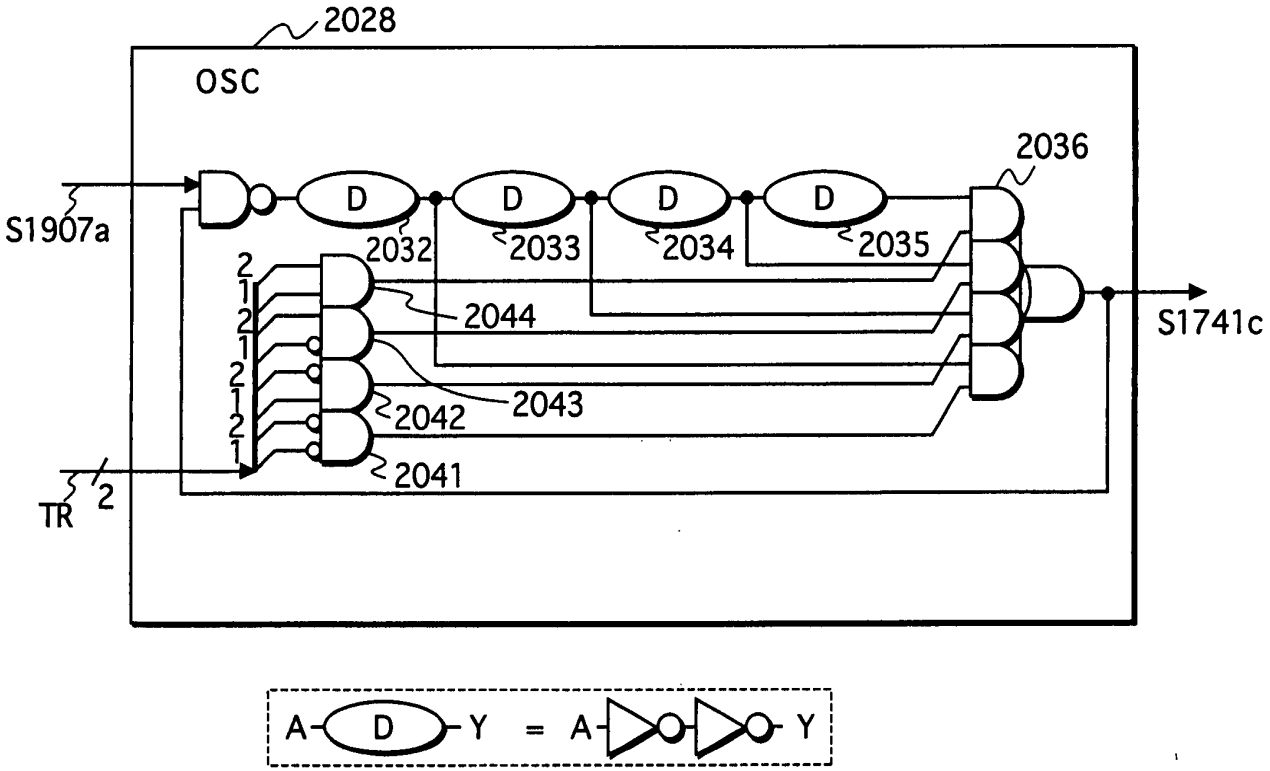

2028
OSC
2036
S1907a
D
D
D
D
2032
2033
2034
2035
2044
2043
2042
2041
S1741c
TR
2
A
D
Y
=
A
Y

FIG.37

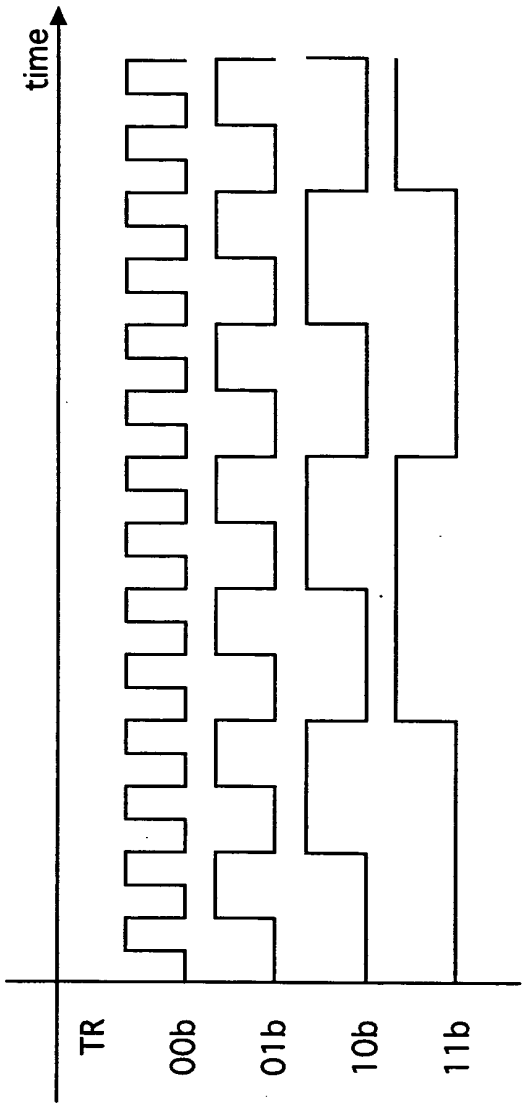


FIG.38

NONVOLATILE MEMORY CELL BLOCK

	SELP	TR	TEST DATA
0000h	1 • • • 1	11 • • • 11	CPU TEST DATA GROUP
0800h	1 • • • 1	01 • • • 01	CPU TEST DATA GROUP
1000h	1 • • • 1	11 • • • 11	D/A TEST DATA GROUP
1800h	1 • • • • 1	01 • • • • 01	TIMER TEST DATA GROUP
	• • •	• • •	• • •

FIG.39

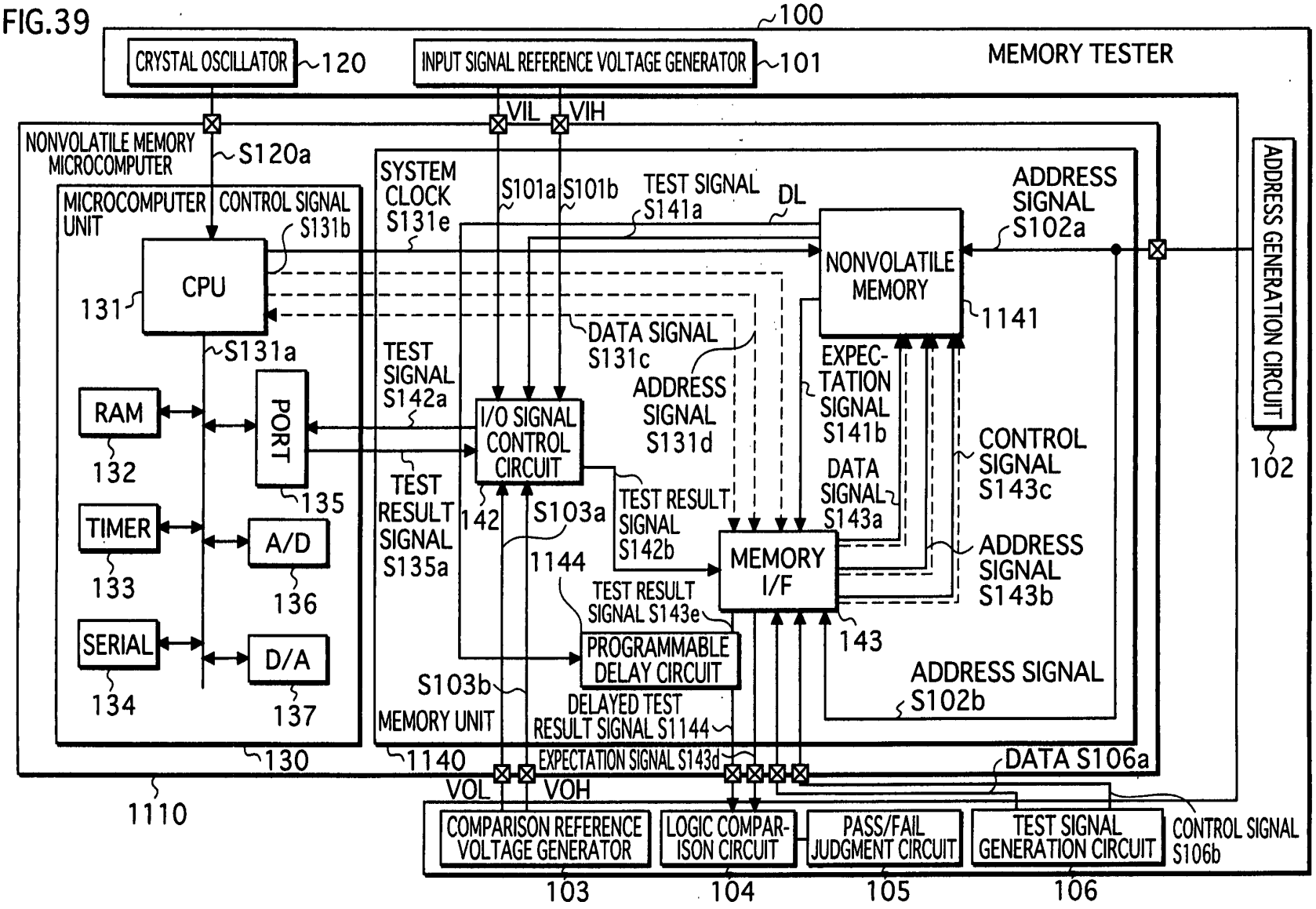

100
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
CPU
131
S131a
RAM
132
PORT
135
TIMER
133
A/D
136
SERIAL
134
D/A
137
130
1110
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
DL
ADDRESS SIGNAL S102a
NONVOLATILE MEMORY
1141
DATA SIGNAL S131c
TEST SIGNAL S142a
ADDRESS SIGNAL S131d
EXPEC-TATION SIGNAL S141b
I/O SIGNAL CONTROL CIRCUIT
CONTROL SIGNAL S143c
DATA SIGNAL S143a
TEST RESULT SIGNAL S135a
142
S103a
TEST RESULT SIGNAL S142b
1144
MEMORY I/F
ADDRESS SIGNAL S143b
TEST RESULT SIGNAL S143e
PROGRAMMABLE DELAY CIRCUIT
143
ADDRESS SIGNAL S102b
S103b
DELAYED TEST RESULT SIGNAL S1144
MEMORY UNIT
1140
EXPECTATION SIGNAL S143d
DATA S106a
VOL
VOH
ADDRESS GENERATION CIRCUIT
102
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPAR-ISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
CONTROL SIGNAL S106b
103
104
105
106

FIG.40

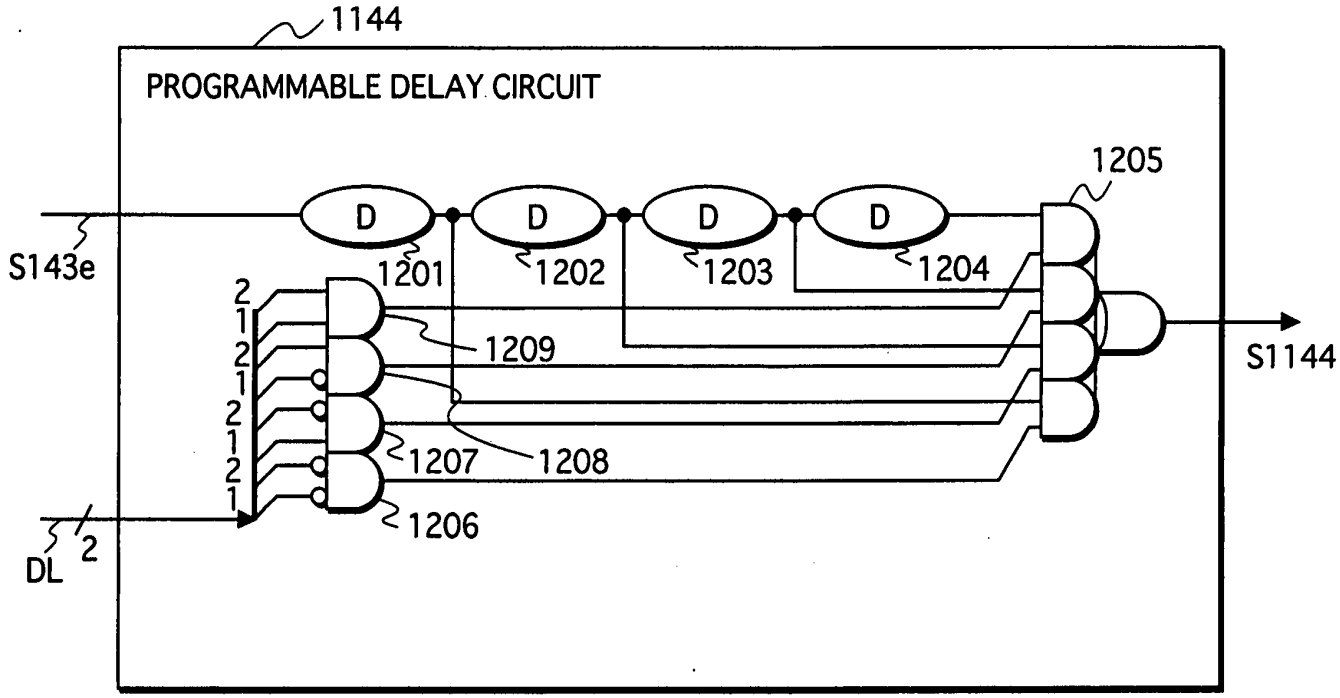

1144
PROGRAMMABLE DELAY CIRCUIT
S143e
D
D
D
D
1201
1202
1203
1204
1205
1209
1207
1208
1206
S1144
DL
2
A
D
Y
=
A
Y

FIG.41

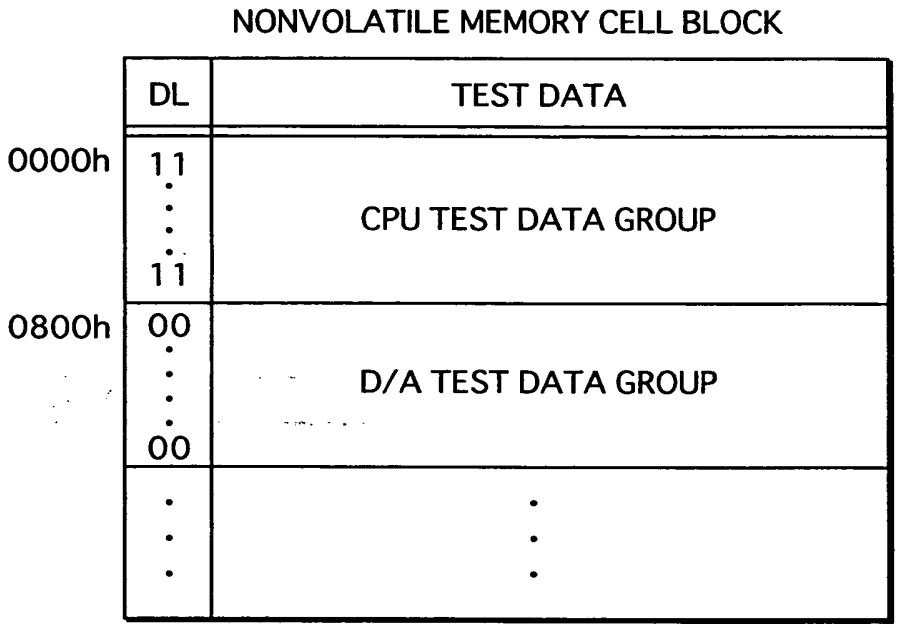

NONVOLATILE MEMORY CELL BLOCK
DL
TEST DATA
0000h
11
11
CPU TEST DATA GROUP
0800h
00
00
D/A TEST DATA GROUP

FIG.42

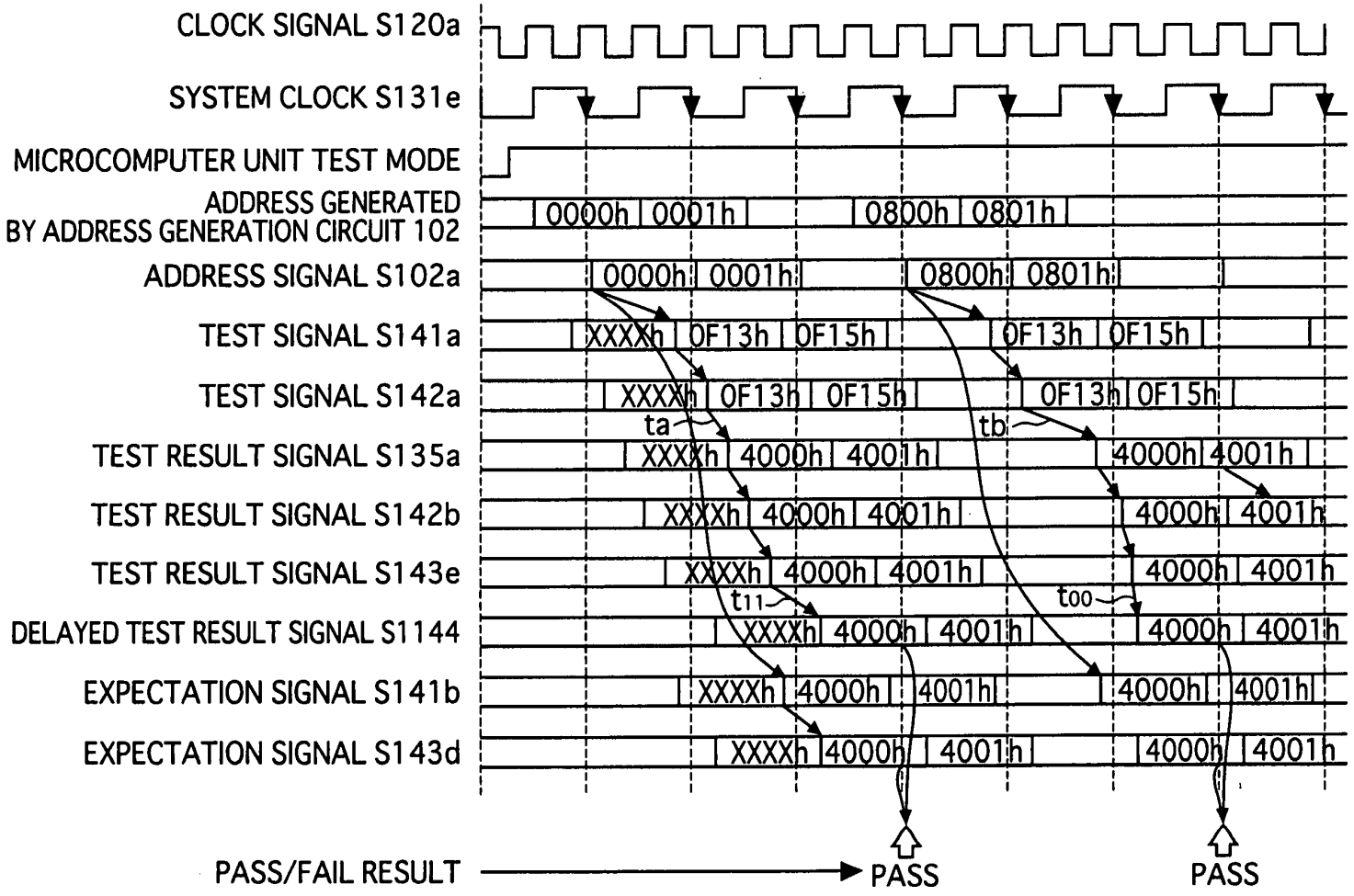

CLOCK SIGNAL S120a
SYSTEM CLOCK S131e
MICROCOMPUTER UNIT TEST MODE
ADDRESS GENERATED BY ADDRESS GENERATION CIRCUIT 102
ADDRESS SIGNAL S102a
TEST SIGNAL S141a
TEST SIGNAL S142a
TEST RESULT SIGNAL S135a
TEST RESULT SIGNAL S142b
TEST RESULT SIGNAL S143e
DELAYED TEST RESULT SIGNAL S1144
EXPECTATION SIGNAL S141b
EXPECTATION SIGNAL S143d
PASS/FAIL RESULT
0000h
0001h
0800h
0801h
XXXXh
0F13h
0F15h
4000h
4001h
ta
tb
t11
too
PASS
PASS

FIG.43

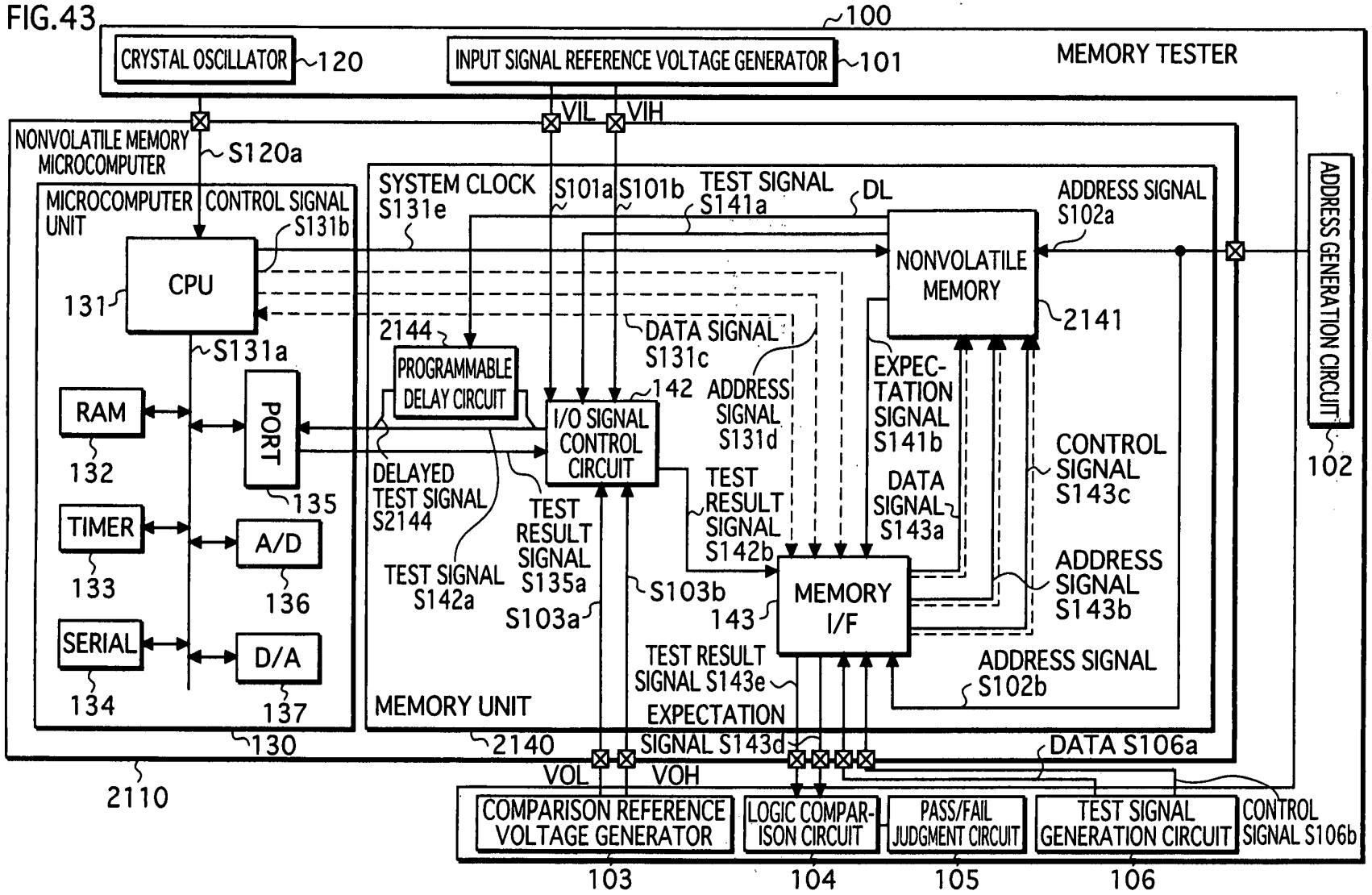
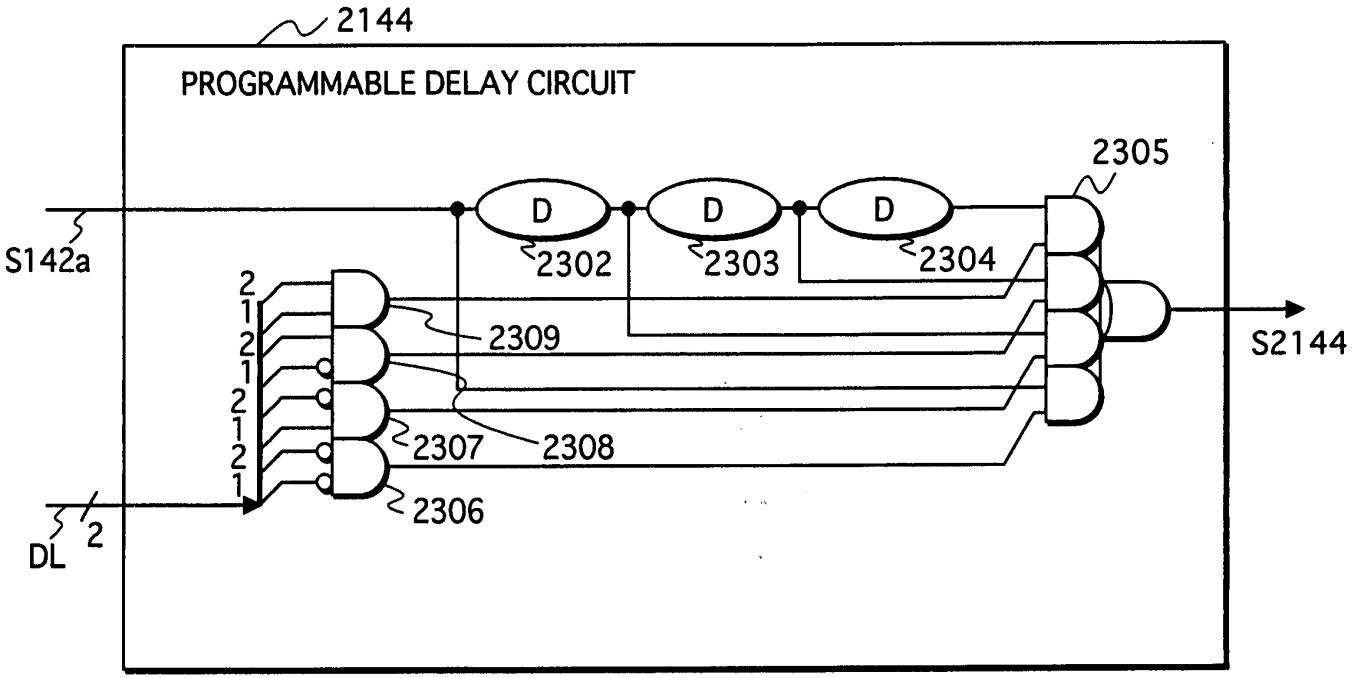

100
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
CPU
131
S131a
RAM
132
PORT
135
TIMER
133
A/D
136
SERIAL
134
D/A
137
130
2110
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
DL
ADDRESS SIGNAL S102a
NONVOLATILE MEMORY
2141
2144
PROGRAMMABLE DELAY CIRCUIT
DATA SIGNAL S131c
142
I/O SIGNAL CONTROL CIRCUIT
ADDRESS SIGNAL S131d
EXPECTATION SIGNAL S141b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
DELAYED TEST SIGNAL S2144
TEST RESULT SIGNAL S135a
TEST RESULT SIGNAL S142b
TEST SIGNAL S142a
S103a
S103b
MEMORY I/F
143
ADDRESS SIGNAL S143b
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL S102b
MEMORY UNIT
2140
EXPECTATION SIGNAL S143d
DATA S106a
VOL
VOH
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
CONTROL SIGNAL S106b
103
104
105
106
ADDRESS GENERATION CIRCUIT
102

FIG.44


2144
PROGRAMMABLE DELAY CIRCUIT
2305
D
D
D
2302
2303
2304
S142a
2309
S2144
2307
2308
2306
DL
2

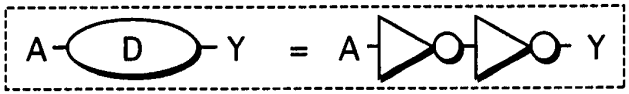

A
D
Y
=
A
Y

FIG.45

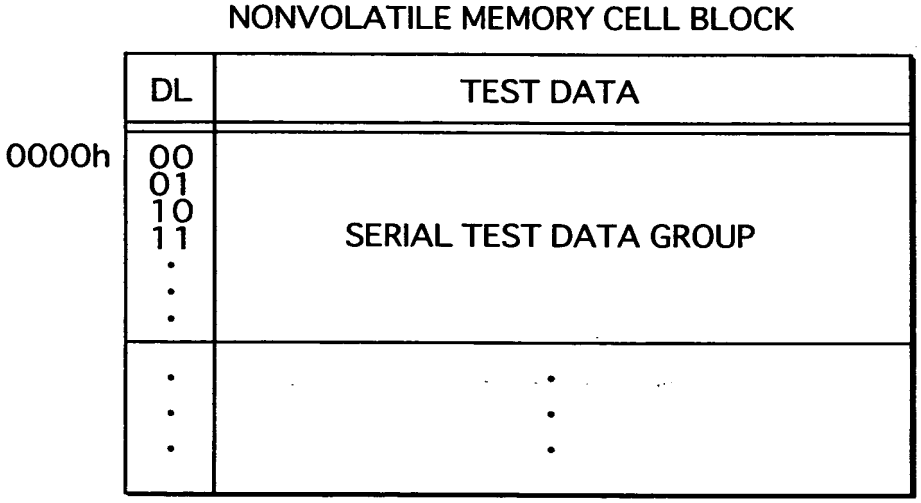

NONVOLATILE MEMORY CELL BLOCK
DL
TEST DATA
0000h
00
01
10
11
SERIAL TEST DATA GROUP

FIG.46

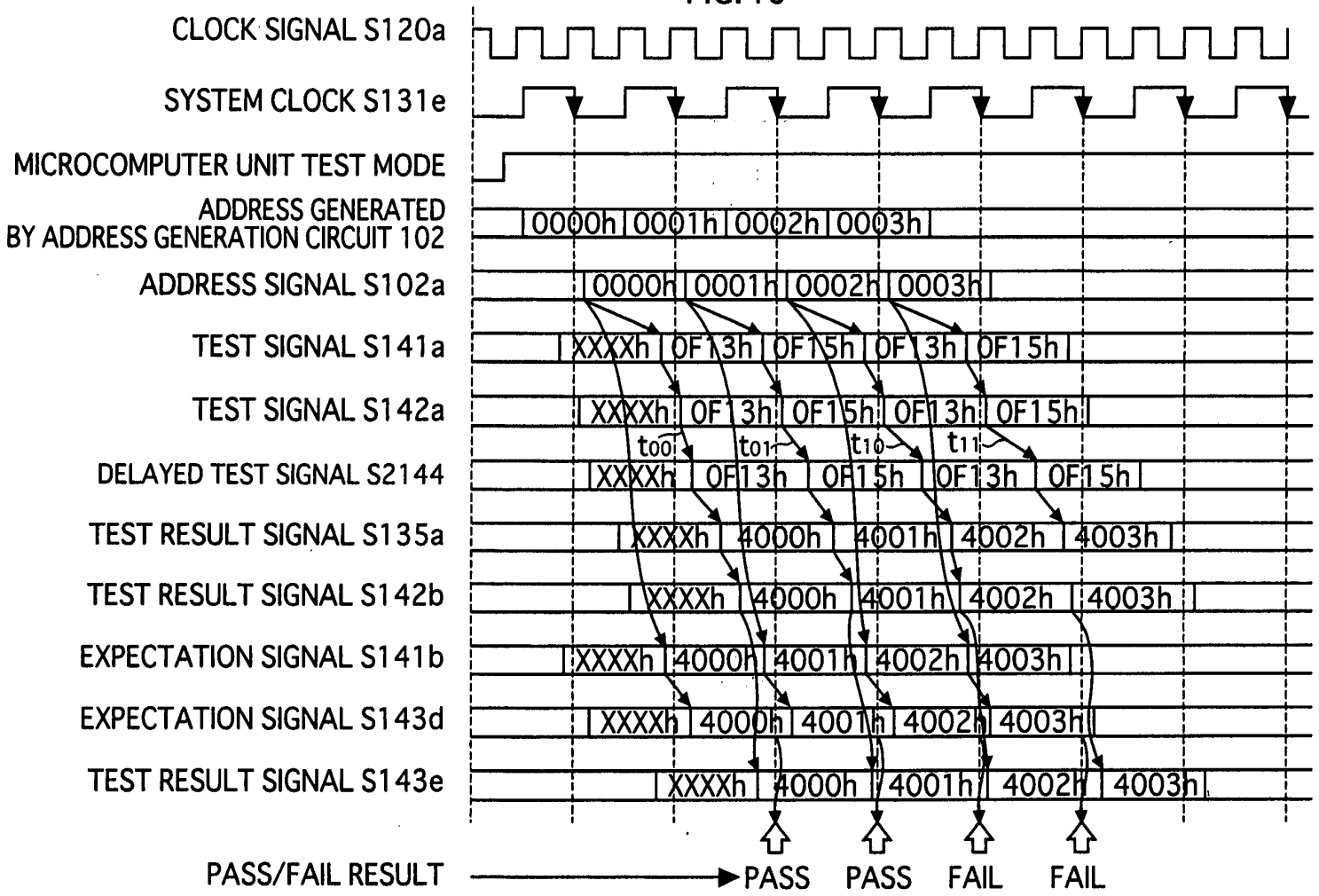

CLOCK SIGNAL S120a
SYSTEM CLOCK S131e
MICROCOMPUTER UNIT TEST MODE
ADDRESS GENERATED BY ADDRESS GENERATION CIRCUIT 102
0000h 0001h 0002h 0003h
ADDRESS SIGNAL S102a
0000h 0001h 0002h 0003h
TEST SIGNAL S141a
XXXXh 0F13h 0F15h 0F13h 0F15h
TEST SIGNAL S142a
XXXXh 0F13h 0F15h 0F13h 0F15h
t00 t01 t10 t11
DELAYED TEST SIGNAL S2144
XXXXh 0F13h 0F15h 0F13h 0F15h
TEST RESULT SIGNAL S135a
XXXXh 4000h 4001h 4002h 4003h
TEST RESULT SIGNAL S142b
XXXXh 4000h 4001h 4002h 4003h
EXPECTATION SIGNAL S141b
XXXXh 4000h 4001h 4002h 4003h
EXPECTATION SIGNAL S143d
XXXXh 4000h 4001h 4002h 4003h
TEST RESULT SIGNAL S143e
XXXXh 4000h 4001h 4002h 4003h
PASS/FAIL RESULT
PASS PASS FAIL FAIL

FIG.47

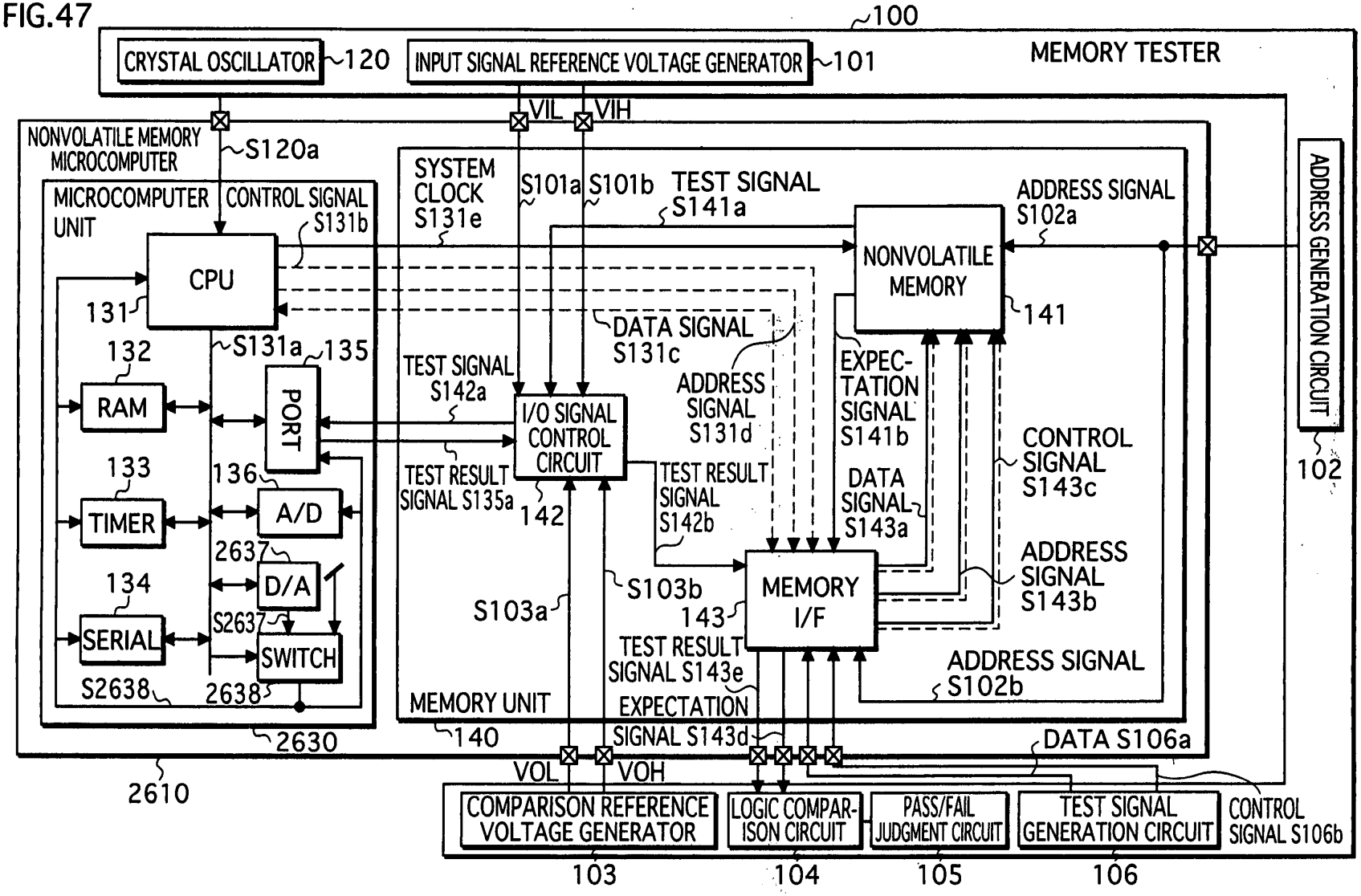

100
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL
S131b
CPU
131
132
RAM
133
TIMER
134
SERIAL
S131a
135
PORT
136
A/D
2637
D/A
S2637
SWITCH
S2638
2638
2630
2610
SYSTEM CLOCK
S131e
S101a
S101b
TEST SIGNAL
S141a
ADDRESS SIGNAL
S102a
NONVOLATILE MEMORY
141
ADDRESS GENERATION CIRCUIT
102
DATA SIGNAL
S131c
TEST SIGNAL
S142a
I/O SIGNAL CONTROL CIRCUIT
ADDRESS SIGNAL
S131d
EXPEC-TATION SIGNAL
S141b
CONTROL SIGNAL
S143c
TEST RESULT SIGNAL S135a
142
TEST RESULT SIGNAL
S142b
DATA SIGNAL
S143a
ADDRESS SIGNAL
S143b
S103a
S103b
143
MEMORY I/F
TEST RESULT SIGNAL S143e
ADDRESS SIGNAL
S102b
MEMORY UNIT
140
EXPECTATION SIGNAL S143d
DATA S106a
VOL
VOH
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPAR-ISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
CONTROL SIGNAL S106b
103
104
105
106

FIG.48

NONVOLATILE MEMORY CELL BLOCK

	SELP	TR	TEST DATA
0000h	1 ... 1	00 ... 00	TEST DATA GROUP USING EXTERNAL POWER
0800h	0 ... 0	01 ... 01	TEST DATA GROUP USING POWER OF FIRST VOLTAGE
1000h	0 ... 0	11 ... 11	TEST DATA GROUP USING POWER OF SECOND VOLTAGE
1800h	0 0 0 0 ...	00 01 10 11 ...	TEST DATA GROUP USING POWER OF VARYING VOLTAGE
...	...	...	...

FIG.49

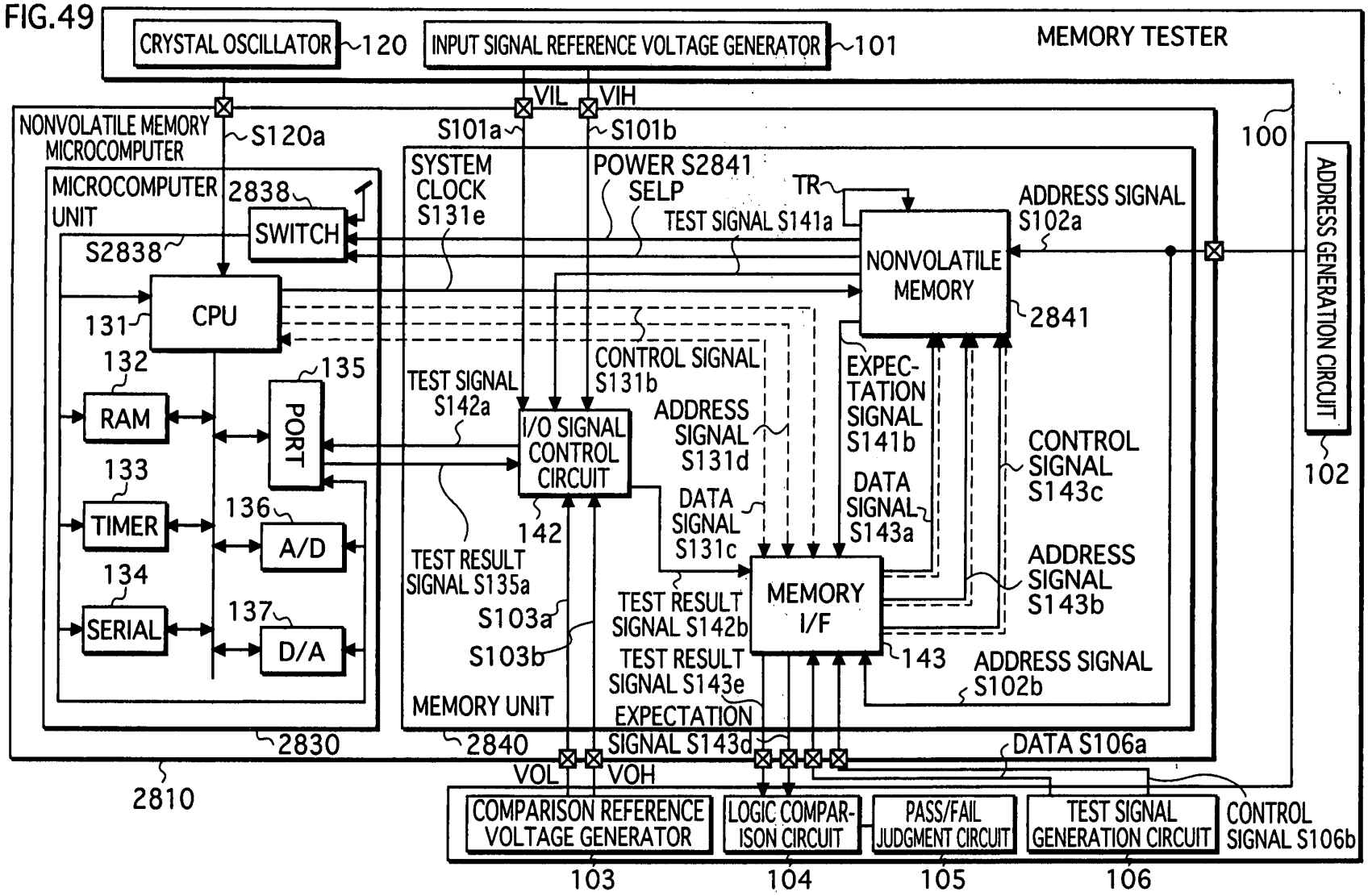

CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
MEMORY TESTER
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
S101a
S101b
100
MICROCOMPUTER UNIT
2838
SWITCH
S2838
SYSTEM CLOCK S131e
POWER S2841
SELP
TR
TEST SIGNAL S141a
ADDRESS SIGNAL S102a
ADDRESS GENERATION CIRCUIT
CPU
131
NONVOLATILE MEMORY
2841
132
135
CONTROL SIGNAL S131b
TEST SIGNAL S142a
EXPEC-TATION SIGNAL S141b
RAM
PORT
I/O SIGNAL CONTROL CIRCUIT
ADDRESS SIGNAL S131d
CONTROL SIGNAL S143c
102
133
136
142
DATA SIGNAL S131c
DATA SIGNAL S143a
TIMER
A/D
TEST RESULT SIGNAL S135a
MEMORY I/F
ADDRESS SIGNAL S143b
134
137
S103a
TEST RESULT SIGNAL S142b
SERIAL
D/A
S103b
TEST RESULT SIGNAL S143e
143
ADDRESS SIGNAL S102b
MEMORY UNIT
EXPECTATION SIGNAL S143d
DATA S106a
2830
2840
VOL
VOH
2810
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPAR-ISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
CONTROL SIGNAL S106b
103
104
105
106

FIG.50

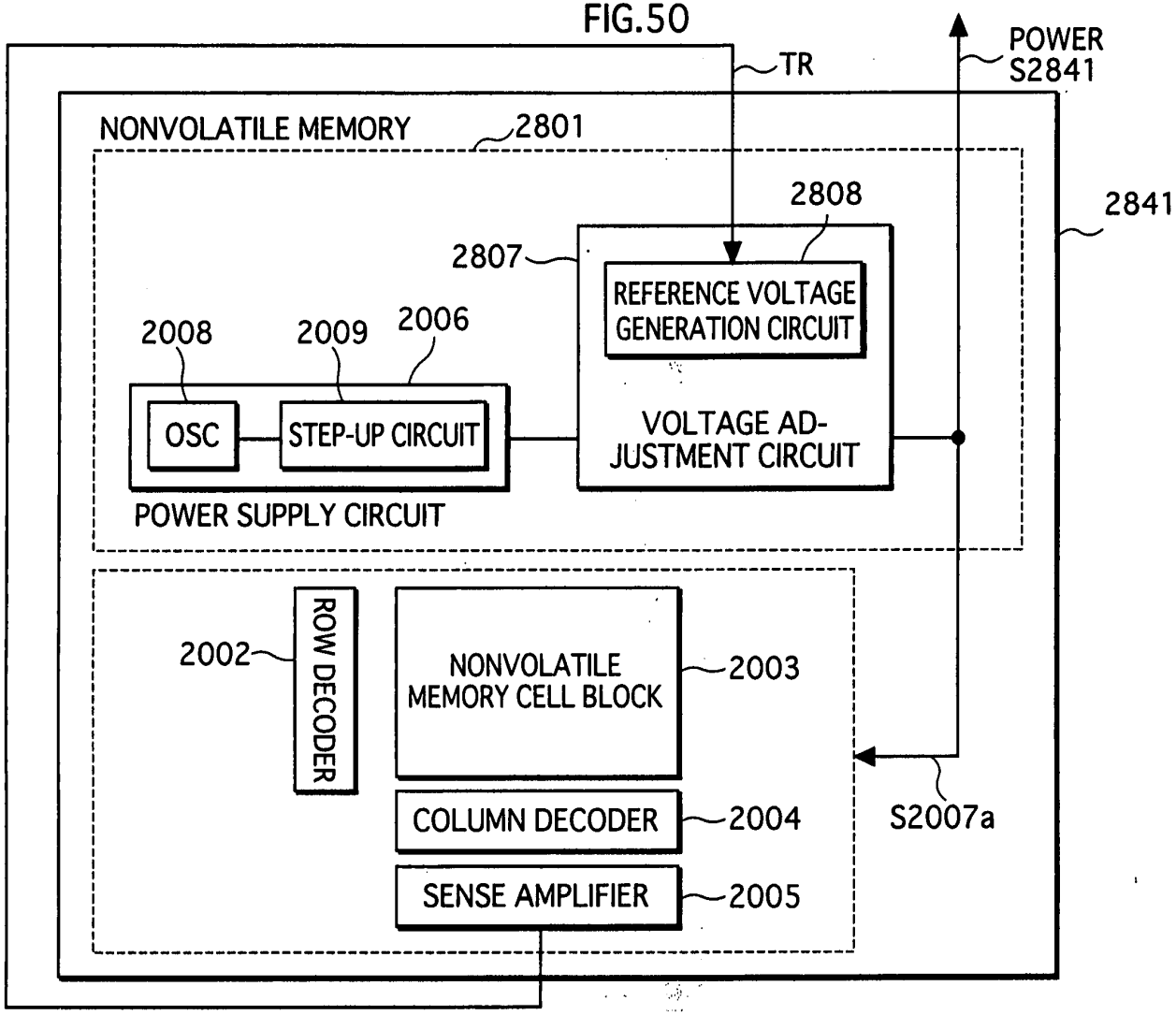

TR
POWER
S2841
NONVOLATILE MEMORY
2801
2841
2808
2807
REFERENCE VOLTAGE GENERATION CIRCUIT
2008
2009
2006
OSC
STEP-UP CIRCUIT
VOLTAGE AD-JUSTMENT CIRCUIT
POWER SUPPLY CIRCUIT
2002
ROW DECODER
NONVOLATILE MEMORY CELL BLOCK
2003
COLUMN DECODER
2004
SENSE AMPLIFIER
2005
S2007a

FIG.51

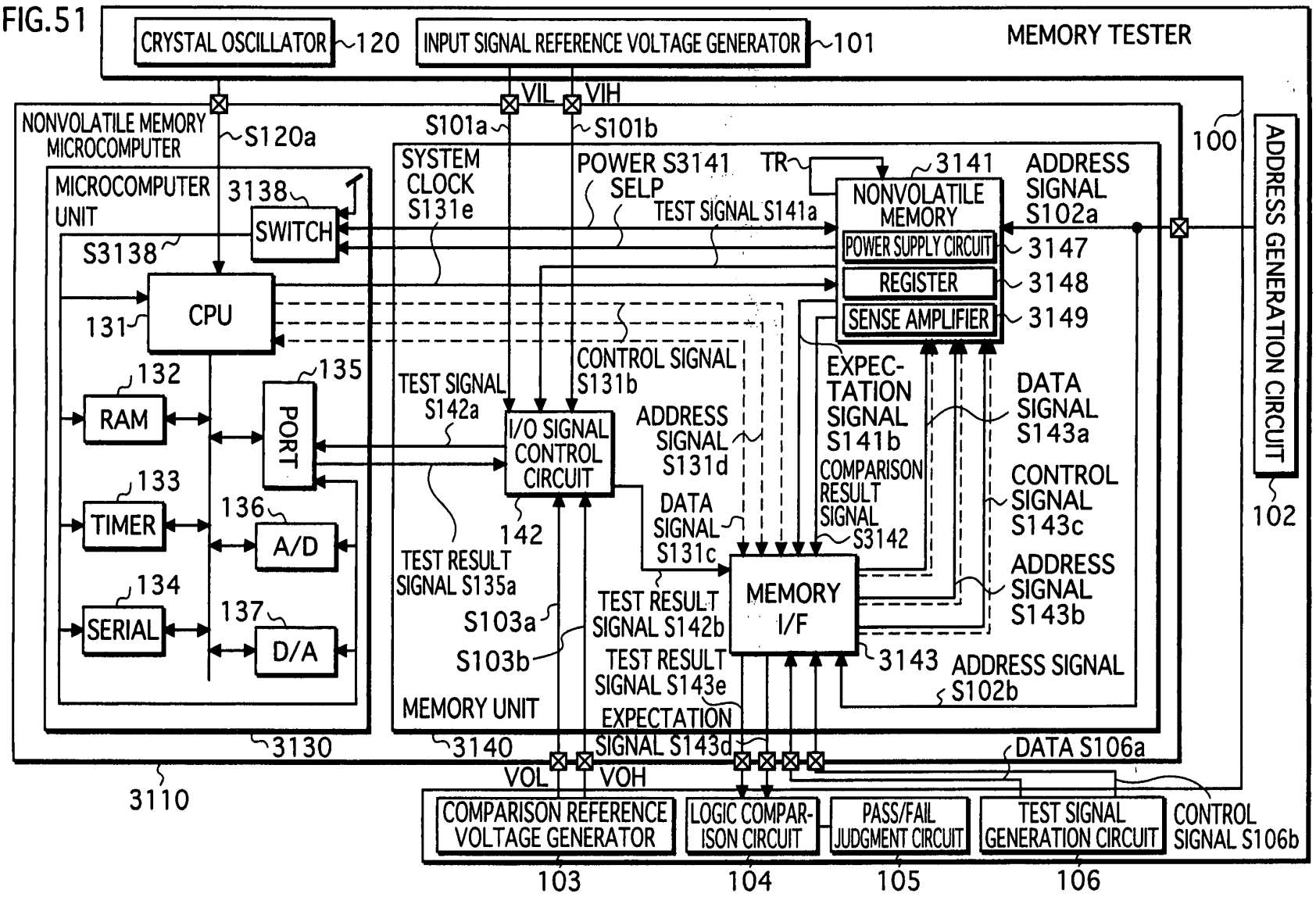

CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
MEMORY TESTER
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
S101a
S101b
100
ADDRESS GENERATION CIRCUIT
SYSTEM CLOCK S131e
POWER S3141
SELP
TR
3141
ADDRESS SIGNAL S102a
MICROCOMPUTER UNIT
3138
SWITCH
TEST SIGNAL S141a
NONVOLATILE MEMORY
POWER SUPPLY CIRCUIT
3147
REGISTER
3148
SENSE AMPLIFIER
3149
S3138
CPU
131
CONTROL SIGNAL S131b
EXPEC-TATION SIGNAL S141b
DATA SIGNAL S143a
132
RAM
135
PORT
TEST SIGNAL S142a
I/O SIGNAL CONTROL CIRCUIT
ADDRESS SIGNAL S131d
COMPARISON RESULT SIGNAL S3142
CONTROL SIGNAL S143c
133
TIMER
136
A/D
142
DATA SIGNAL S131c
TEST RESULT SIGNAL S135a
MEMORY I/F
ADDRESS SIGNAL S143b
134
SERIAL
137
D/A
S103a
TEST RESULT SIGNAL S142b
S103b
TEST RESULT SIGNAL S143e
3143
ADDRESS SIGNAL S102b
MEMORY UNIT
EXPECTATION SIGNAL S143d
DATA S106a
102
3130
3140
3110
VOL
VOH
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPAR-ISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
CONTROL SIGNAL S106b
103
104
105
106

FIG.52

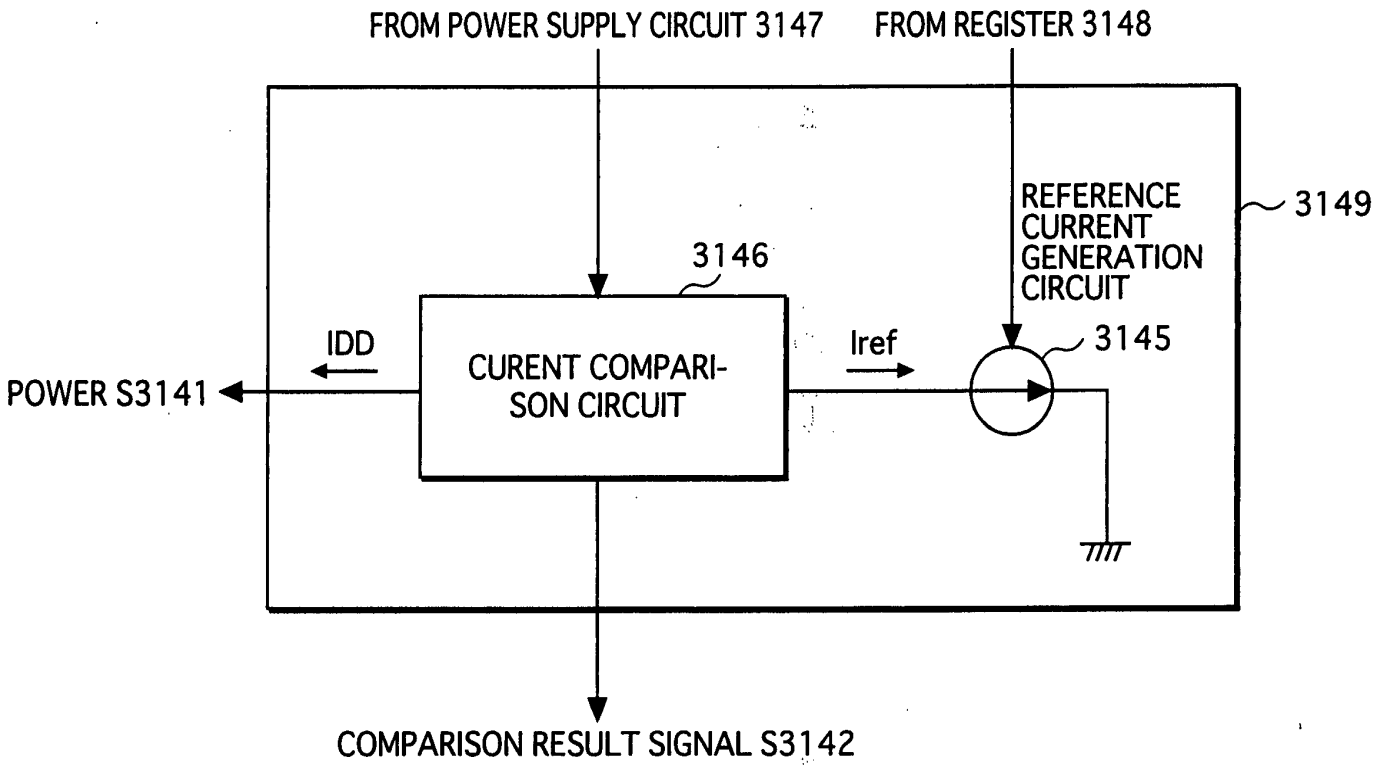

FROM POWER SUPPLY CIRCUIT 3147
FROM REGISTER 3148
REFERENCE CURRENT GENERATION CIRCUIT
3149
3146
IDD
CURENT COMPARI-SON CIRCUIT
Iref
3145
POWER S3141
COMPARISON RESULT SIGNAL S3142

FIG.53

NONVOLATILE MEMORY CELL BLOCK

	SELP	TR	TEST DATA
0000h	1 • • • 1	00 • • • 00	TEST DATA GROUP WITHOUT CURRENT STANDARD
0800h	0 • • • 0	01 • • • 01	TEST DATA GROUP WITH STOP CURRENT STANDARD
1000h	0 • • • 0	11 • • • 11	TEST DATA GROUP WITH OPERATING CURRENT STANDARD
	• • •	• • •	• • •

FIG.54

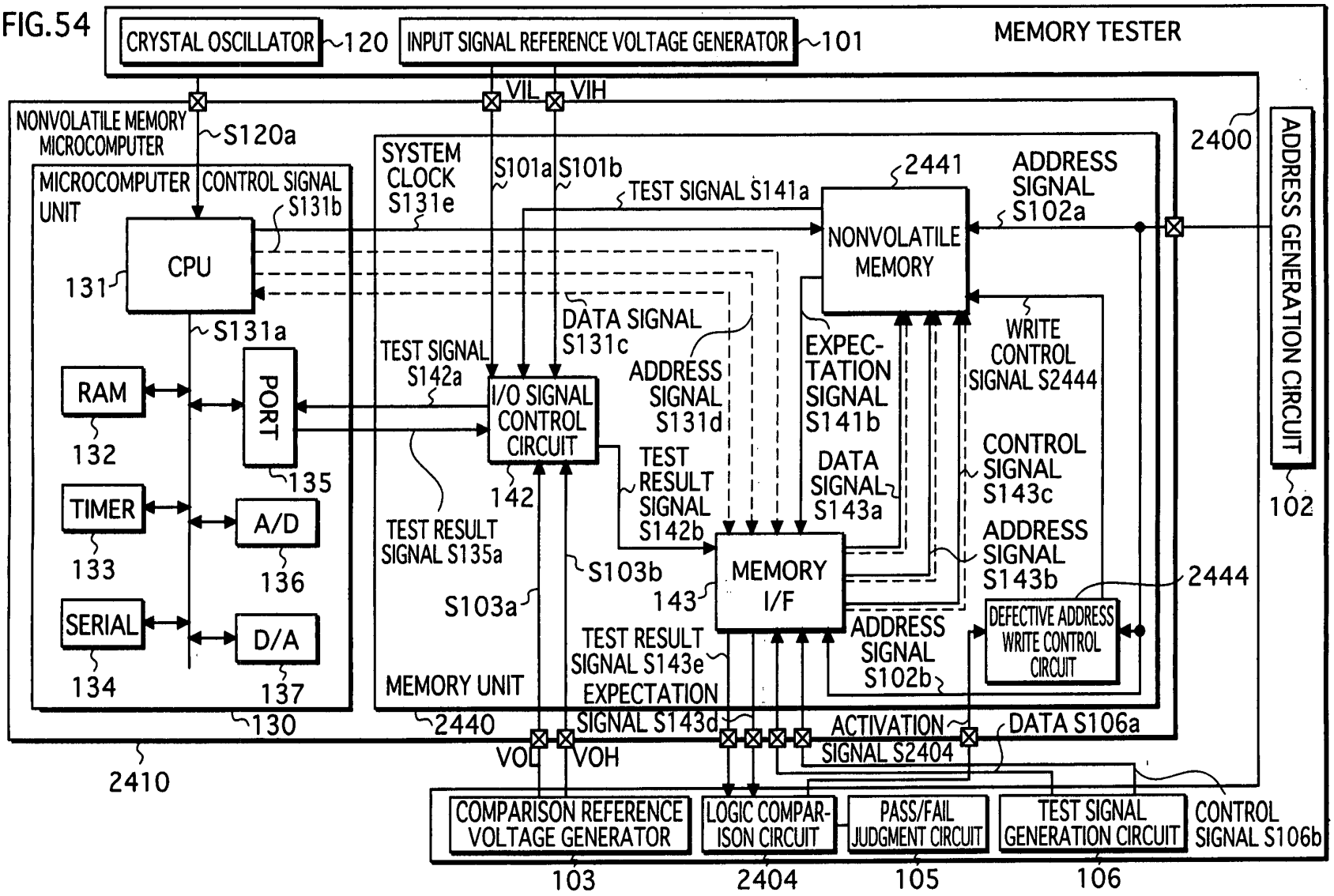

CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
MEMORY TESTER
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
2400
ADDRESS GENERATION CIRCUIT
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
2441
ADDRESS SIGNAL S102a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
NONVOLATILE MEMORY
CPU
131
S131a
DATA SIGNAL S131c
WRITE CONTROL SIGNAL S2444
TEST SIGNAL S142a
ADDRESS SIGNAL S131d
EXPECTATION SIGNAL S141b
RAM
132
PORT
135
I/O SIGNAL CONTROL CIRCUIT
142
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
TIMER
133
A/D
136
TEST RESULT SIGNAL S135a
ADDRESS SIGNAL S143b
2444
S103b
MEMORY I/F
143
S103a
SERIAL
134
D/A
137
TEST RESULT SIGNAL S143e
DEFECTIVE ADDRESS WRITE CONTROL CIRCUIT
ADDRESS SIGNAL S102b
MEMORY UNIT
EXPECTATION SIGNAL S143d
ACTIVATION SIGNAL S2404
DATA S106a
130
2440
102
VOL
VOH
2410
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
CONTROL SIGNAL S106b
103
2404
105
106

FIG.55A

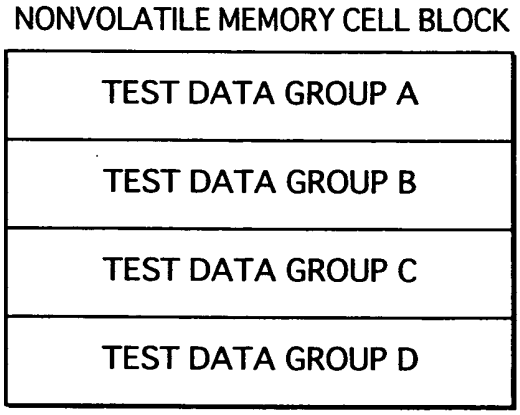


FIG.55B

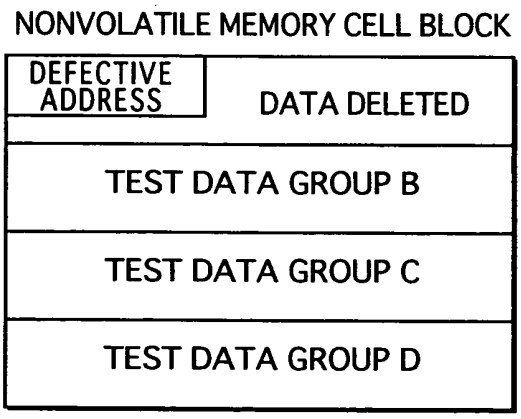


FIG.56

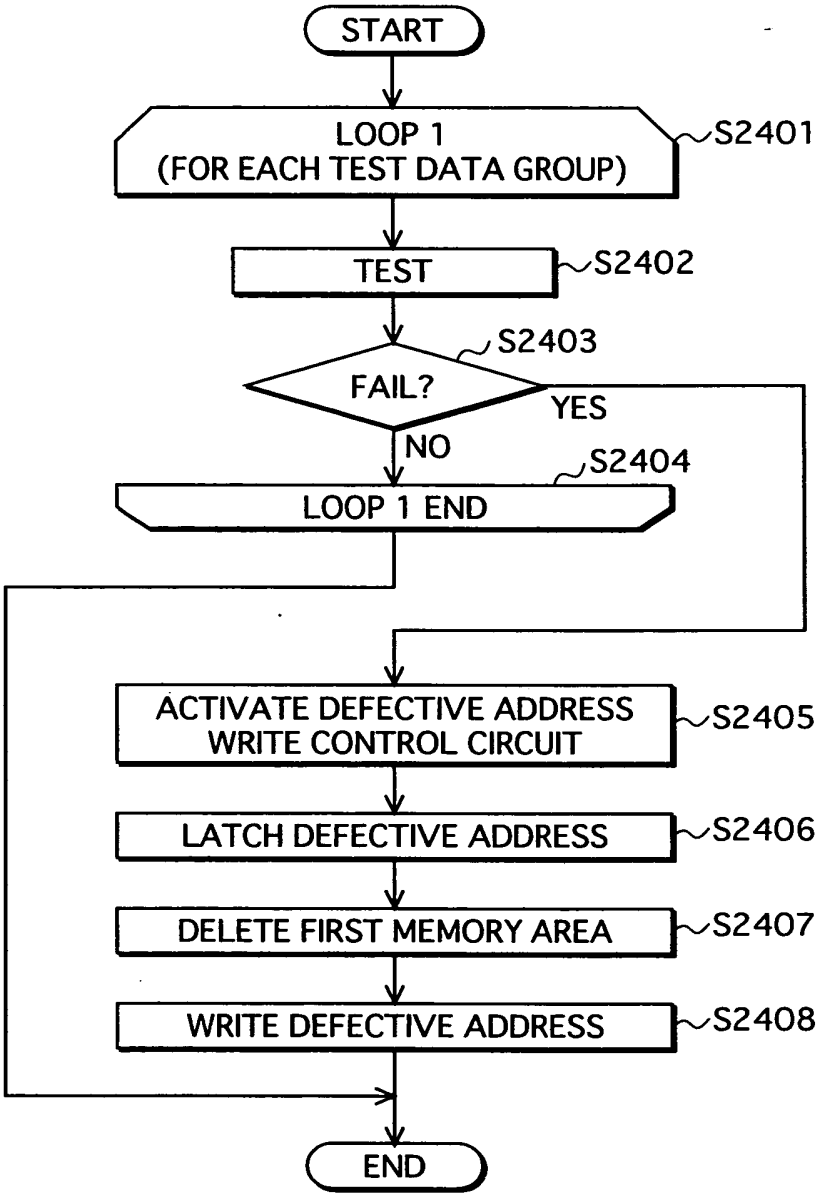

START
LOOP 1
(FOR EACH TEST DATA GROUP)
S2401
TEST
S2402
S2403
FAIL?
YES
NO
S2404
LOOP 1 END
ACTIVATE DEFECTIVE ADDRESS
WRITE CONTROL CIRCUIT
S2405
LATCH DEFECTIVE ADDRESS
S2406
DELETE FIRST MEMORY AREA
S2407
WRITE DEFECTIVE ADDRESS
S2408
END

FIG.57

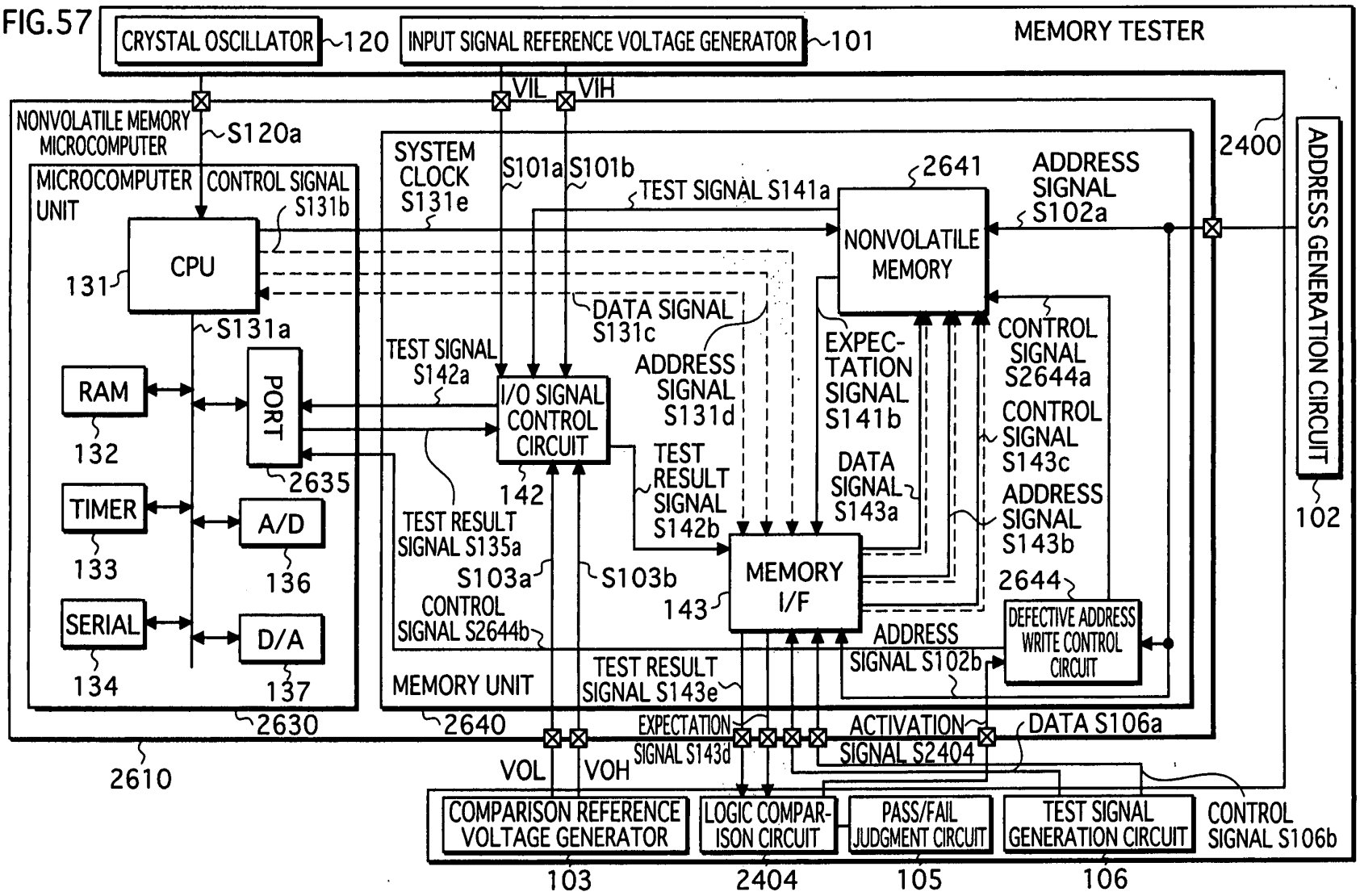

CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
MEMORY TESTER
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
SYSTEM CLOCK S131e
S101a
S101b
2400
ADDRESS GENERATION CIRCUIT
2641
ADDRESS SIGNAL S102a
TEST SIGNAL S141a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
NONVOLATILE MEMORY
CPU
131
S131a
DATA SIGNAL S131c
CONTROL SIGNAL S2644a
TEST SIGNAL S142a
ADDRESS SIGNAL S131d
EXPECTATION SIGNAL S141b
CONTROL SIGNAL S143c
RAM
132
PORT
2635
I/O SIGNAL CONTROL CIRCUIT
142
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
ADDRESS SIGNAL S143b
TIMER
133
A/D
136
TEST RESULT SIGNAL S135a
S103a
S103b
MEMORY I/F
143
2644
SERIAL
134
D/A
137
CONTROL SIGNAL S2644b
ADDRESS SIGNAL S102b
DEFECTIVE ADDRESS WRITE CONTROL CIRCUIT
TEST RESULT SIGNAL S143e
MEMORY UNIT
2630
2640
EXPECTATION SIGNAL S143d
ACTIVATION SIGNAL S2404
DATA S106a
2610
VOL
VOH
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
CONTROL SIGNAL S106b
103
2404
105
106
102

FIG.58A

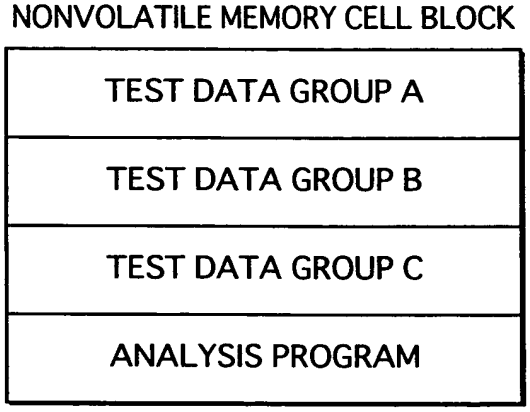


FIG.58B

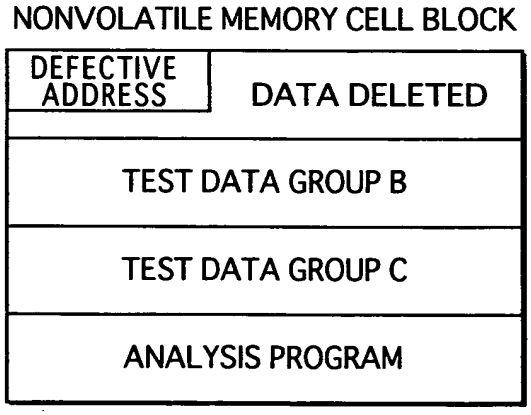


FIG.59

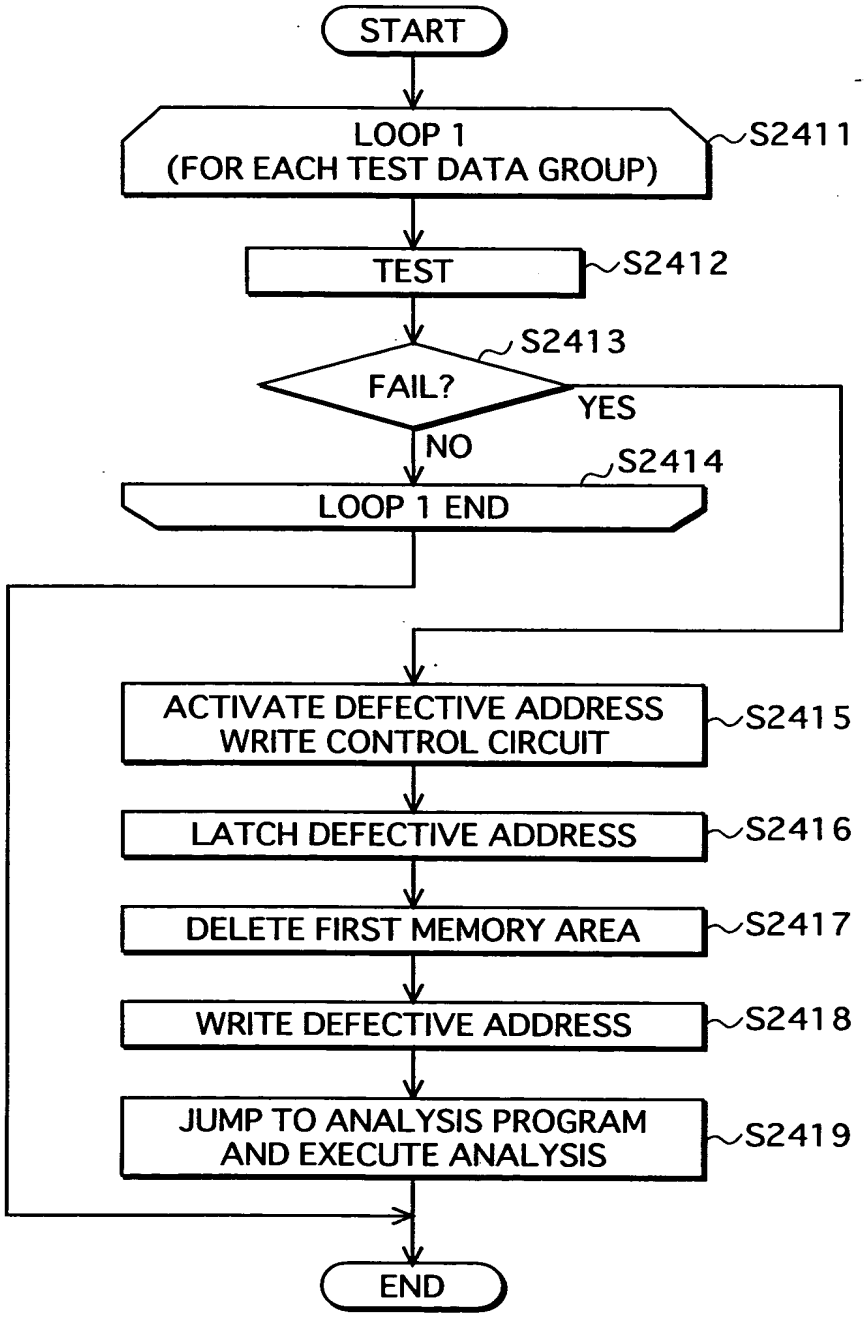

START
LOOP 1
(FOR EACH TEST DATA GROUP)
S2411
TEST
S2412
S2413
FAIL?
YES
NO
S2414
LOOP 1 END
ACTIVATE DEFECTIVE ADDRESS WRITE CONTROL CIRCUIT
S2415
LATCH DEFECTIVE ADDRESS
S2416
DELETE FIRST MEMORY AREA
S2417
WRITE DEFECTIVE ADDRESS
S2418
JUMP TO ANALYSIS PROGRAM AND EXECUTE ANALYSIS
S2419
END

FIG.60

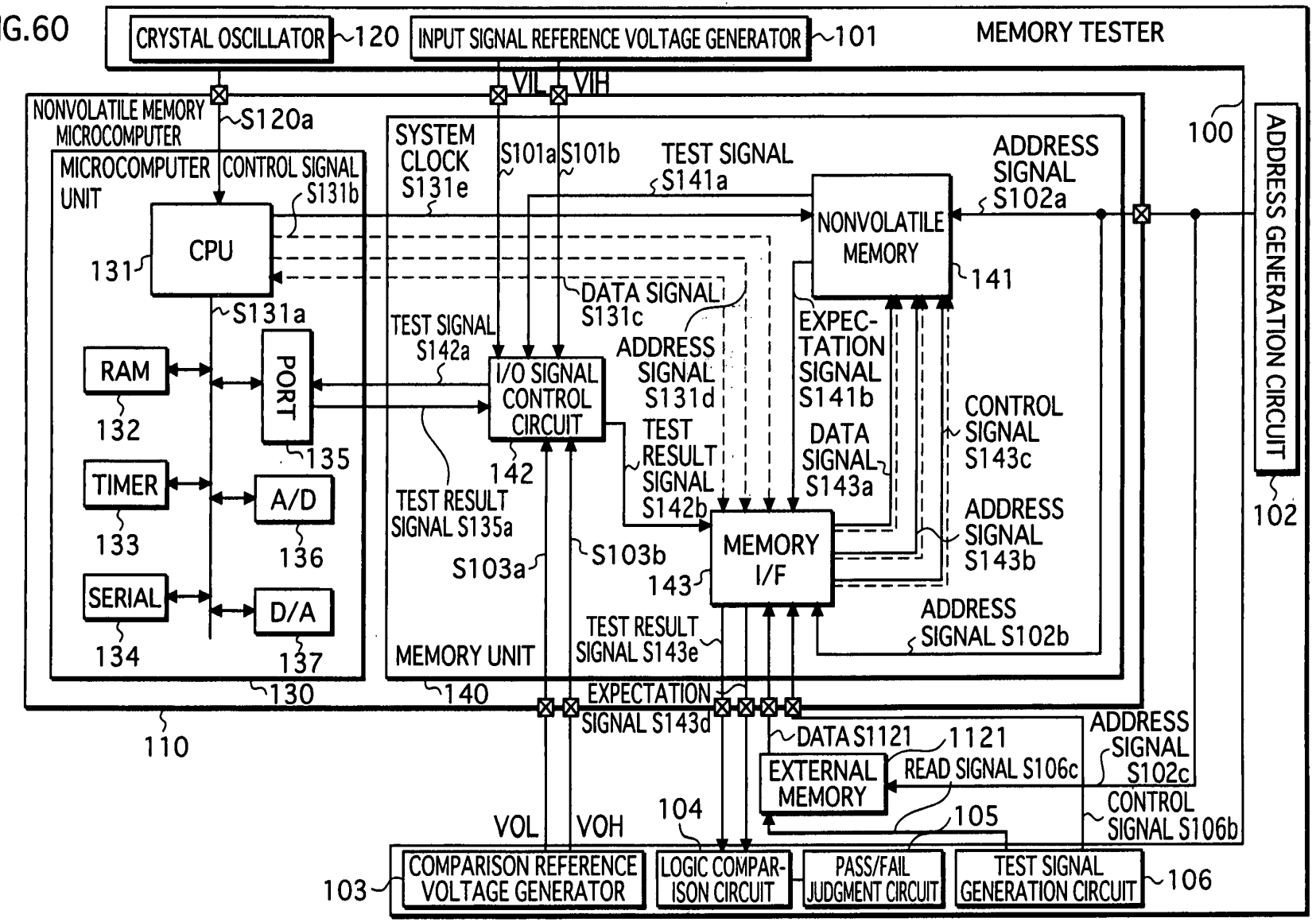

CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
MEMORY TESTER
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL
S131b
CPU
131
S131a
RAM
132
PORT
135
TIMER
133
A/D
136
SERIAL
134
D/A
137
130
110
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
NONVOLATILE MEMORY
141
ADDRESS SIGNAL S102a
100
ADDRESS GENERATION CIRCUIT
102
DATA SIGNAL S131c
TEST SIGNAL S142a
I/O SIGNAL CONTROL CIRCUIT
142
ADDRESS SIGNAL S131d
EXPECTATION SIGNAL S141b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
ADDRESS SIGNAL S143b
TEST RESULT SIGNAL S142b
TEST RESULT SIGNAL S135a
S103a
S103b
MEMORY I/F
143
ADDRESS SIGNAL S102b
TEST RESULT SIGNAL S143e
MEMORY UNIT
140
EXPECTATION SIGNAL S143d
DATA S1121
1121
EXTERNAL MEMORY
READ SIGNAL S106c
ADDRESS SIGNAL S102c
CONTROL SIGNAL S106b
VOL
VOH
104
105
103
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
106

FIG.61

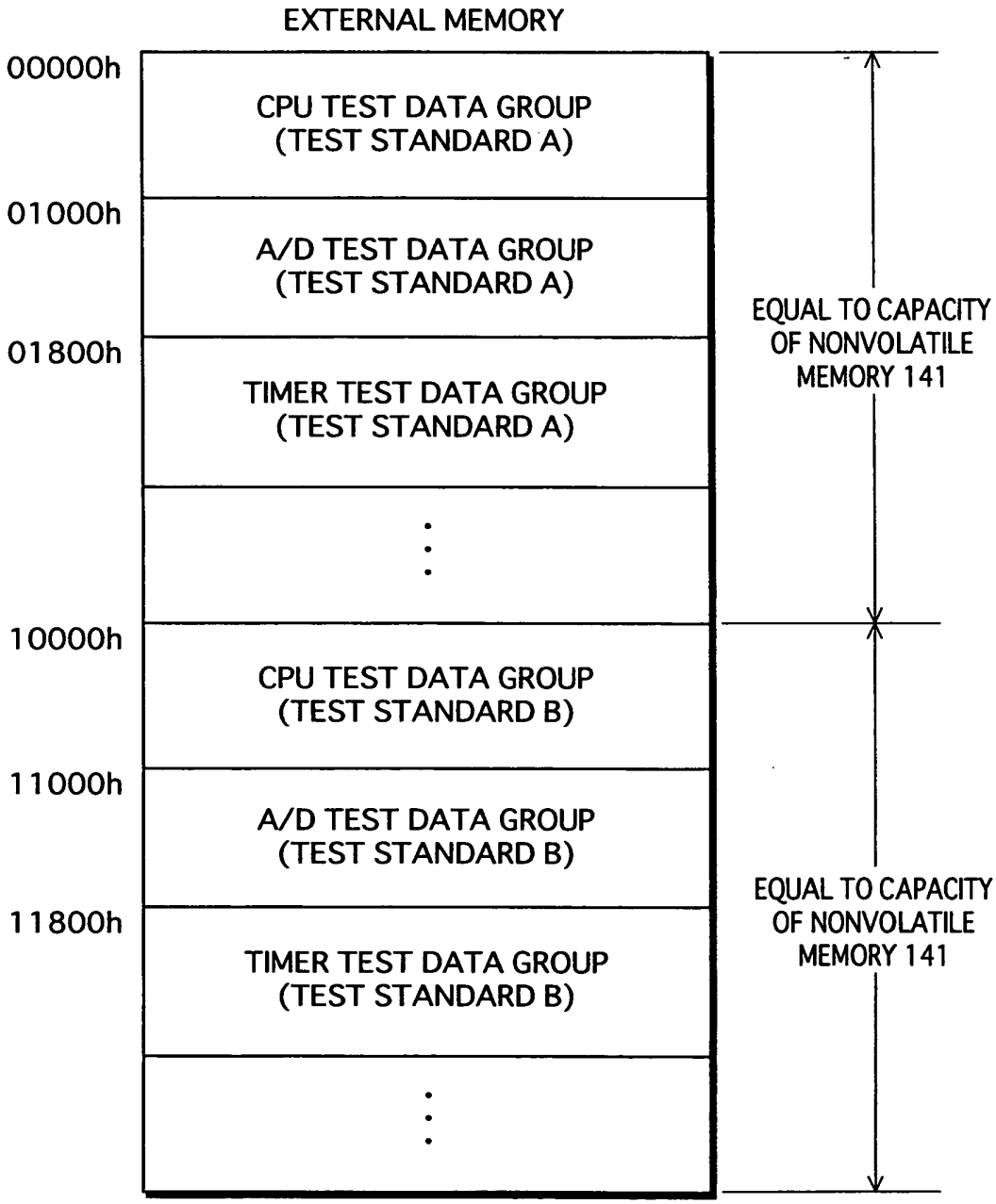

EXTERNAL MEMORY
00000h
CPU TEST DATA GROUP
(TEST STANDARD A)
01000h
A/D TEST DATA GROUP
(TEST STANDARD A)
01800h
TIMER TEST DATA GROUP
(TEST STANDARD A)
EQUAL TO CAPACITY
OF NONVOLATILE
MEMORY 141
10000h
CPU TEST DATA GROUP
(TEST STANDARD B)
11000h
A/D TEST DATA GROUP
(TEST STANDARD B)
11800h
TIMER TEST DATA GROUP
(TEST STANDARD B)
EQUAL TO CAPACITY
OF NONVOLATILE
MEMORY 141

FIG.62

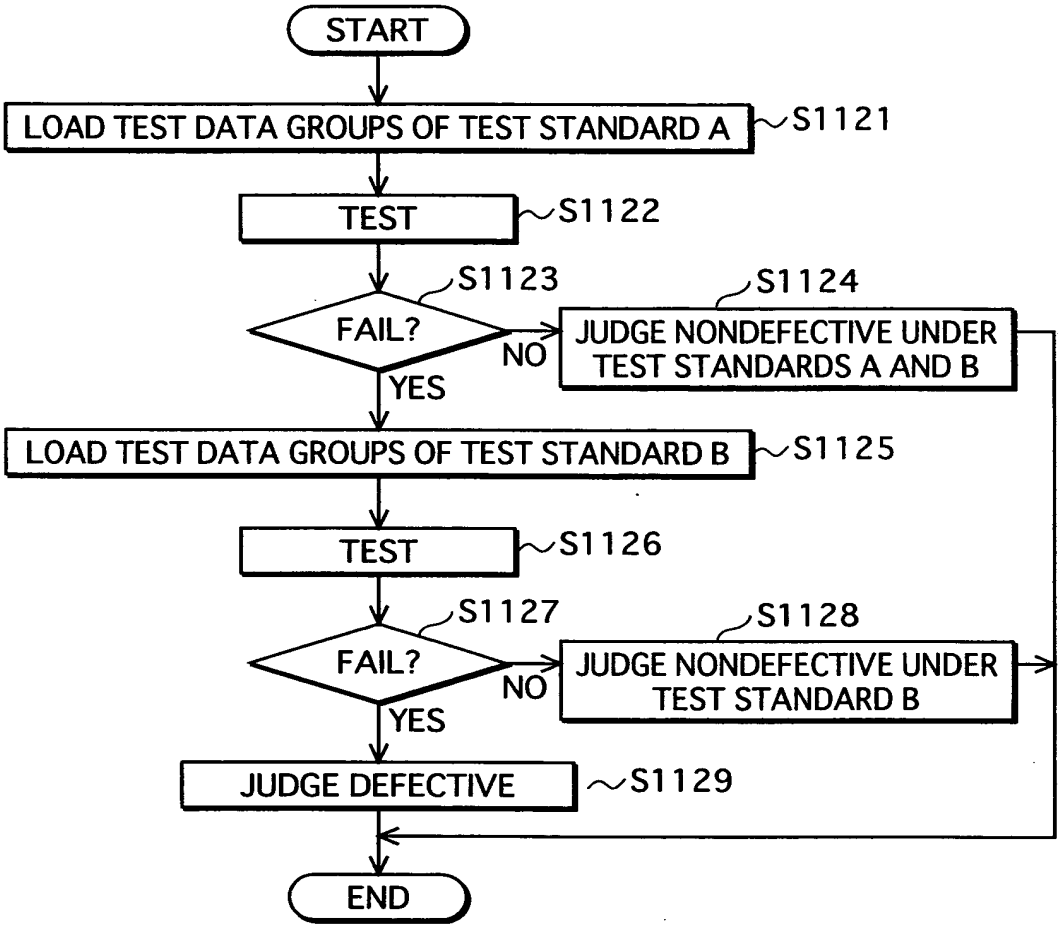

START
LOAD TEST DATA GROUPS OF TEST STANDARD A
S1121
TEST
S1122
S1123
FAIL?
NO
S1124
JUDGE NONDEFECTIVE UNDER TEST STANDARDS A AND B
YES
LOAD TEST DATA GROUPS OF TEST STANDARD B
S1125
TEST
S1126
S1127
FAIL?
NO
S1128
JUDGE NONDEFECTIVE UNDER TEST STANDARD B
YES
JUDGE DEFECTIVE
S1129
END

FIG.63

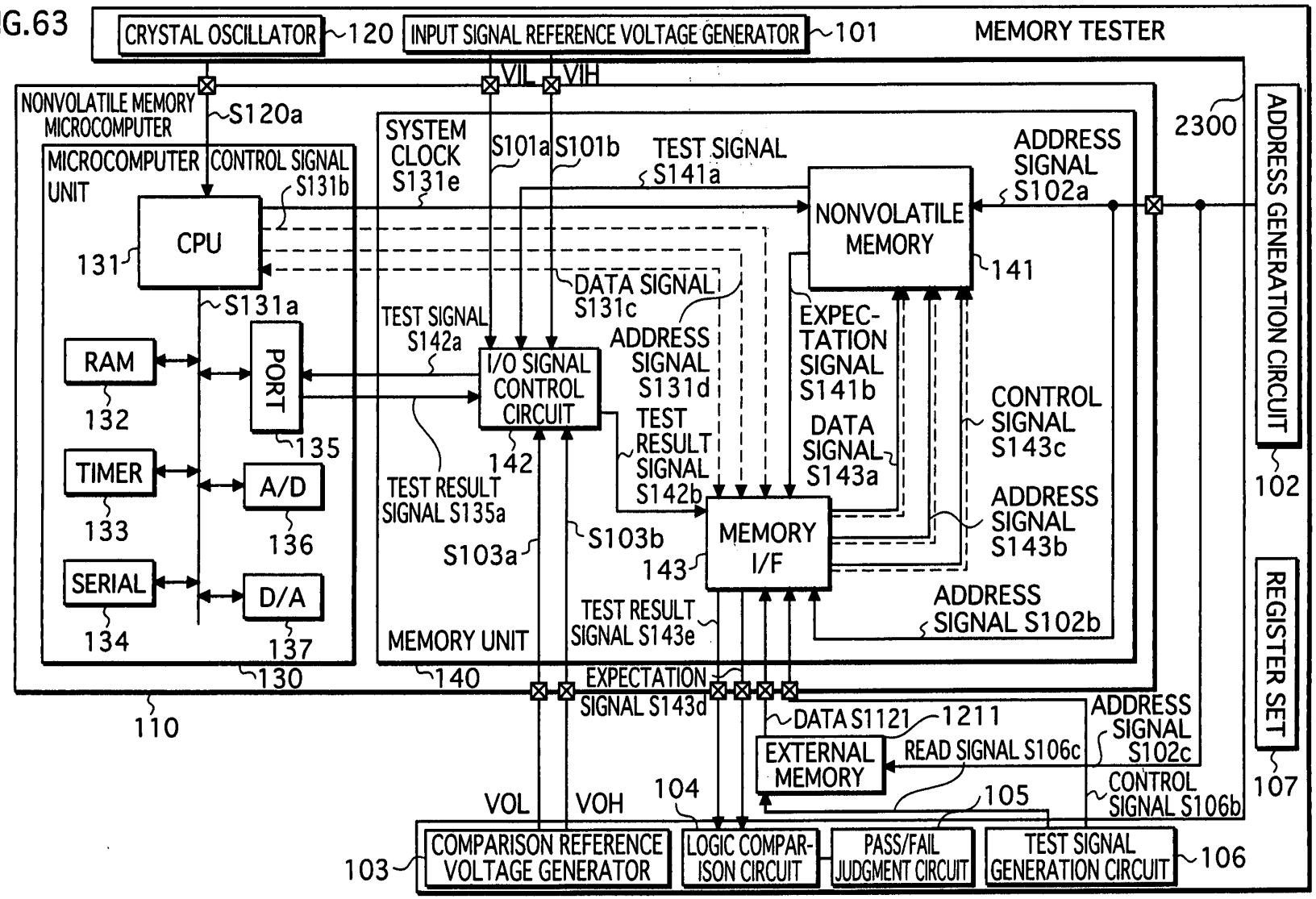

CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
MEMORY TESTER
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
CPU
131
S131a
RAM
132
PORT
135
TIMER
133
A/D
136
SERIAL
134
D/A
137
130
110
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
ADDRESS SIGNAL S102a
2300
ADDRESS GENERATION CIRCUIT
102
NONVOLATILE MEMORY
141
DATA SIGNAL S131c
TEST SIGNAL S142a
I/O SIGNAL CONTROL CIRCUIT
142
ADDRESS SIGNAL S131d
EXPEC-TATION SIGNAL S141b
DATA SIGNAL S143a
CONTROL SIGNAL S143c
TEST RESULT SIGNAL S142b
TEST RESULT SIGNAL S135a
S103a
S103b
MEMORY I/F
143
ADDRESS SIGNAL S143b
ADDRESS SIGNAL S102b
TEST RESULT SIGNAL S143e
MEMORY UNIT
140
EXPECTATION SIGNAL S143d
DATA S1121
1211
ADDRESS SIGNAL S102c
EXTERNAL MEMORY
READ SIGNAL S106c
REGISTER SET
107
CONTROL SIGNAL S106b
VOL
VOH
104
105
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPAR-ISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
106
103

FIG.65

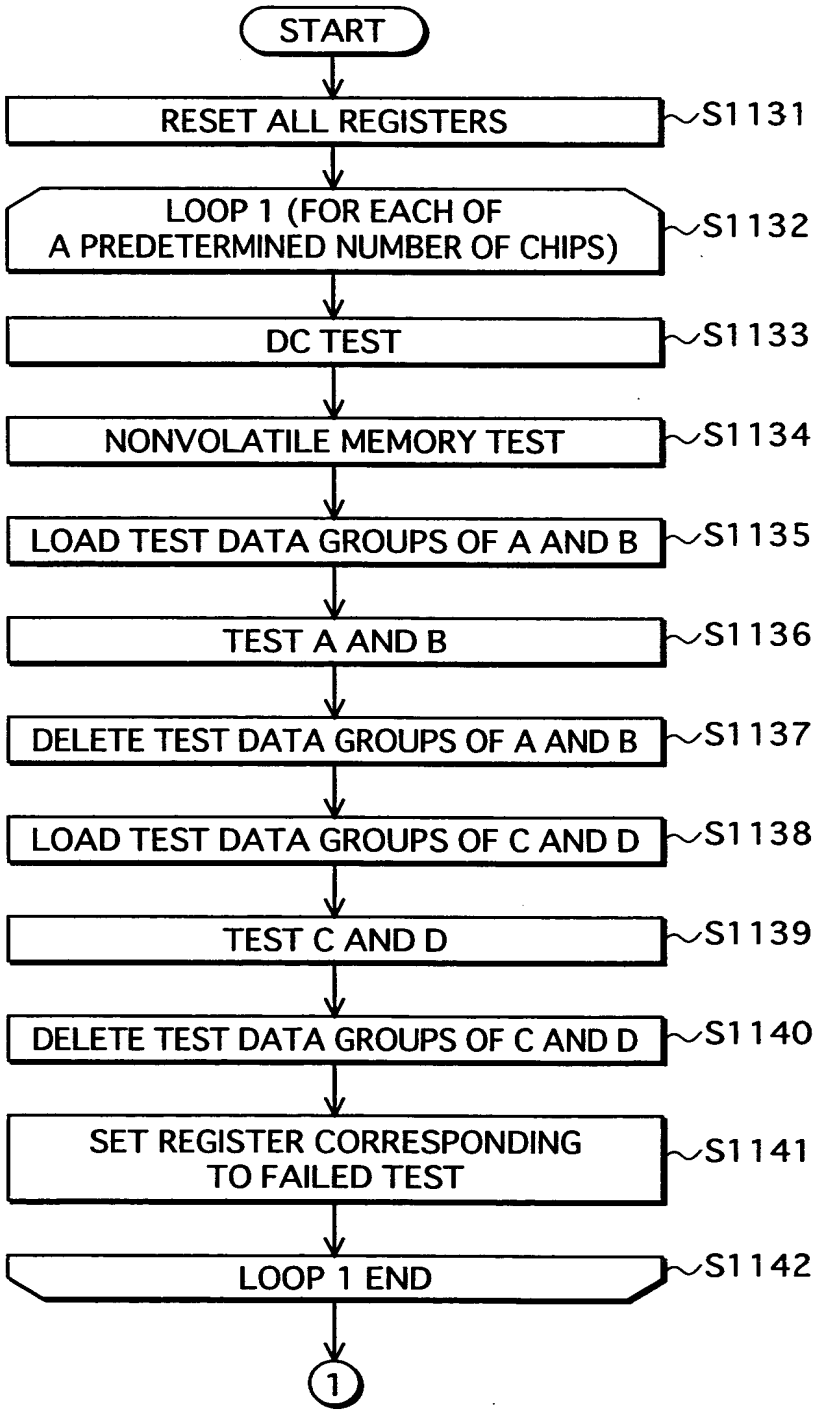

START
RESET ALL REGISTERS
S1131
LOOP 1 (FOR EACH OF A PREDETERMINED NUMBER OF CHIPS)
S1132
DC TEST
S1133
NONVOLATILE MEMORY TEST
S1134
LOAD TEST DATA GROUPS OF A AND B
S1135
TEST A AND B
S1136
DELETE TEST DATA GROUPS OF A AND B
S1137
LOAD TEST DATA GROUPS OF C AND D
S1138
TEST C AND D
S1139
DELETE TEST DATA GROUPS OF C AND D
S1140
SET REGISTER CORRESPONDING TO FAILED TEST
S1141
LOOP 1 END
S1142
1

FIG.64

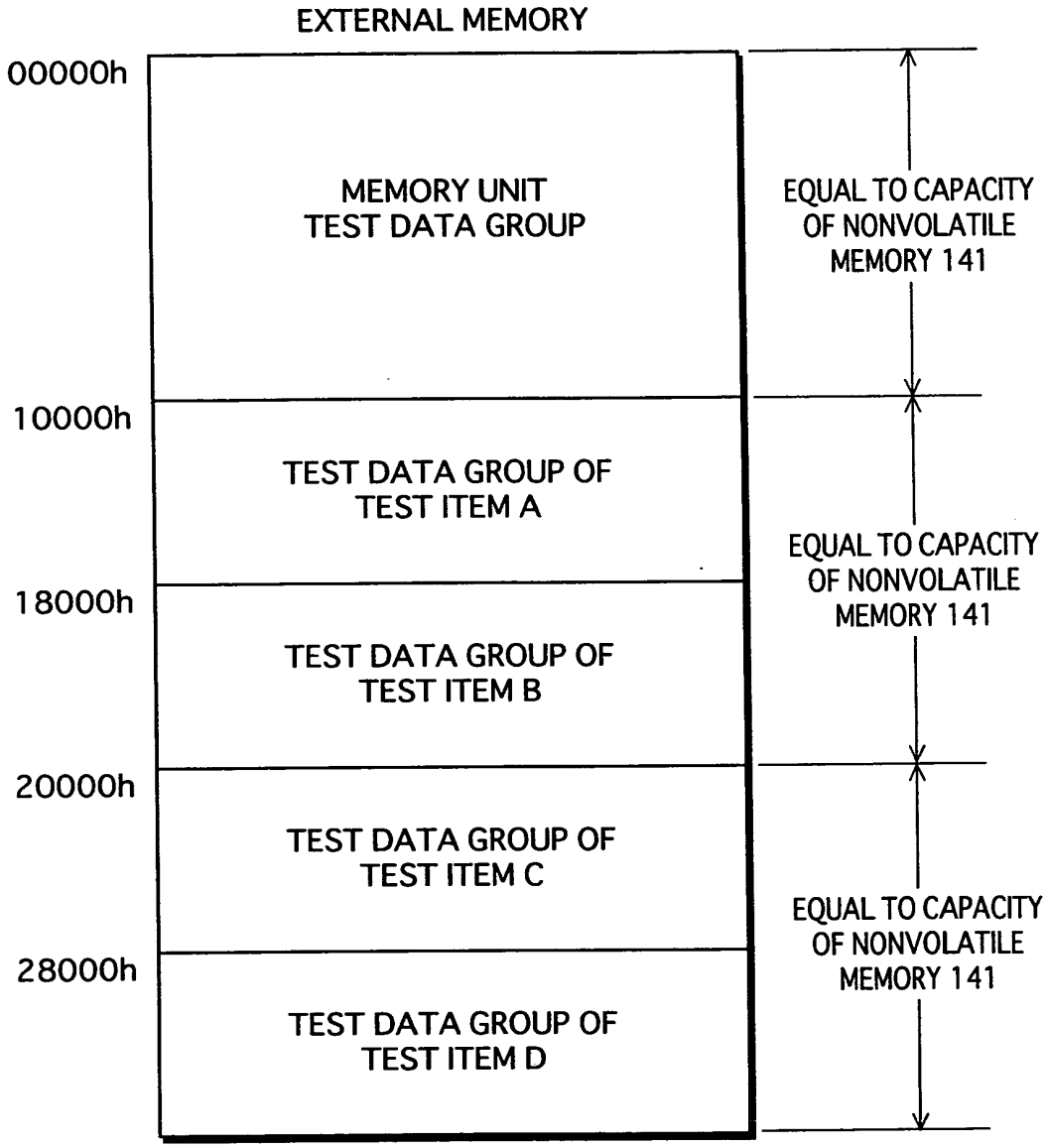

EXTERNAL MEMORY
00000h
10000h
18000h
20000h
28000h
MEMORY UNIT
TEST DATA GROUP
TEST DATA GROUP OF
TEST ITEM A
TEST DATA GROUP OF
TEST ITEM B
TEST DATA GROUP OF
TEST ITEM C
TEST DATA GROUP OF
TEST ITEM D
EQUAL TO CAPACITY
OF NONVOLATILE
MEMORY 141
EQUAL TO CAPACITY
OF NONVOLATILE
MEMORY 141
EQUAL TO CAPACITY
OF NONVOLATILE
MEMORY 141

FIG.66

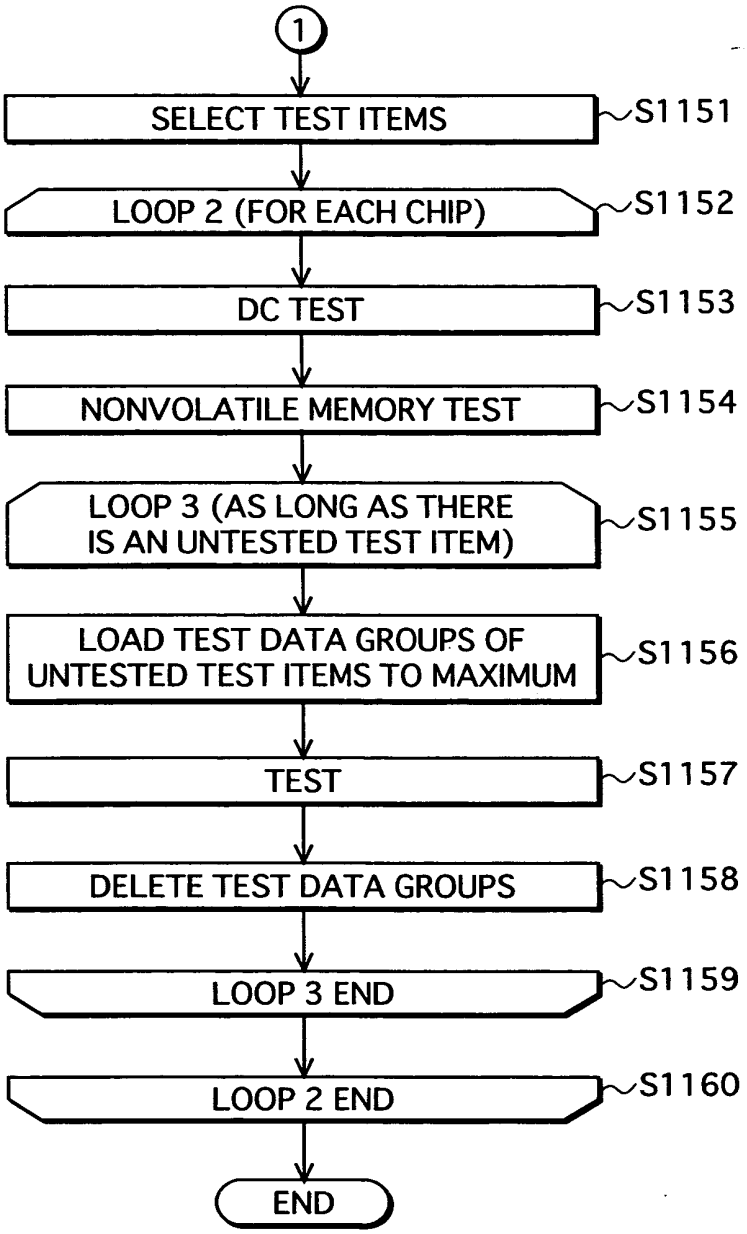

1
SELECT TEST ITEMS
S1151
LOOP 2 (FOR EACH CHIP)
S1152
DC TEST
S1153
NONVOLATILE MEMORY TEST
S1154
LOOP 3 (AS LONG AS THERE IS AN UNTESTED TEST ITEM)
S1155
LOAD TEST DATA GROUPS OF UNTESTED TEST ITEMS TO MAXIMUM
S1156
TEST
S1157
DELETE TEST DATA GROUPS
S1158
LOOP 3 END
S1159
LOOP 2 END
S1160
END

FIG.68A

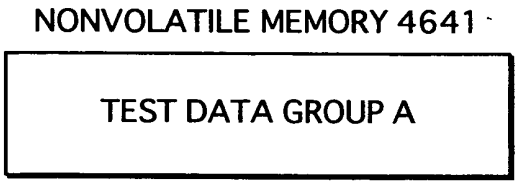


FIG.68B

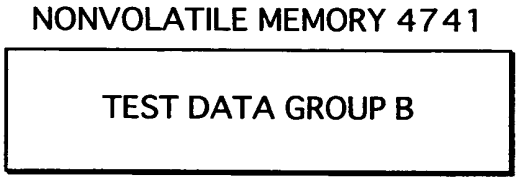


FIG.67

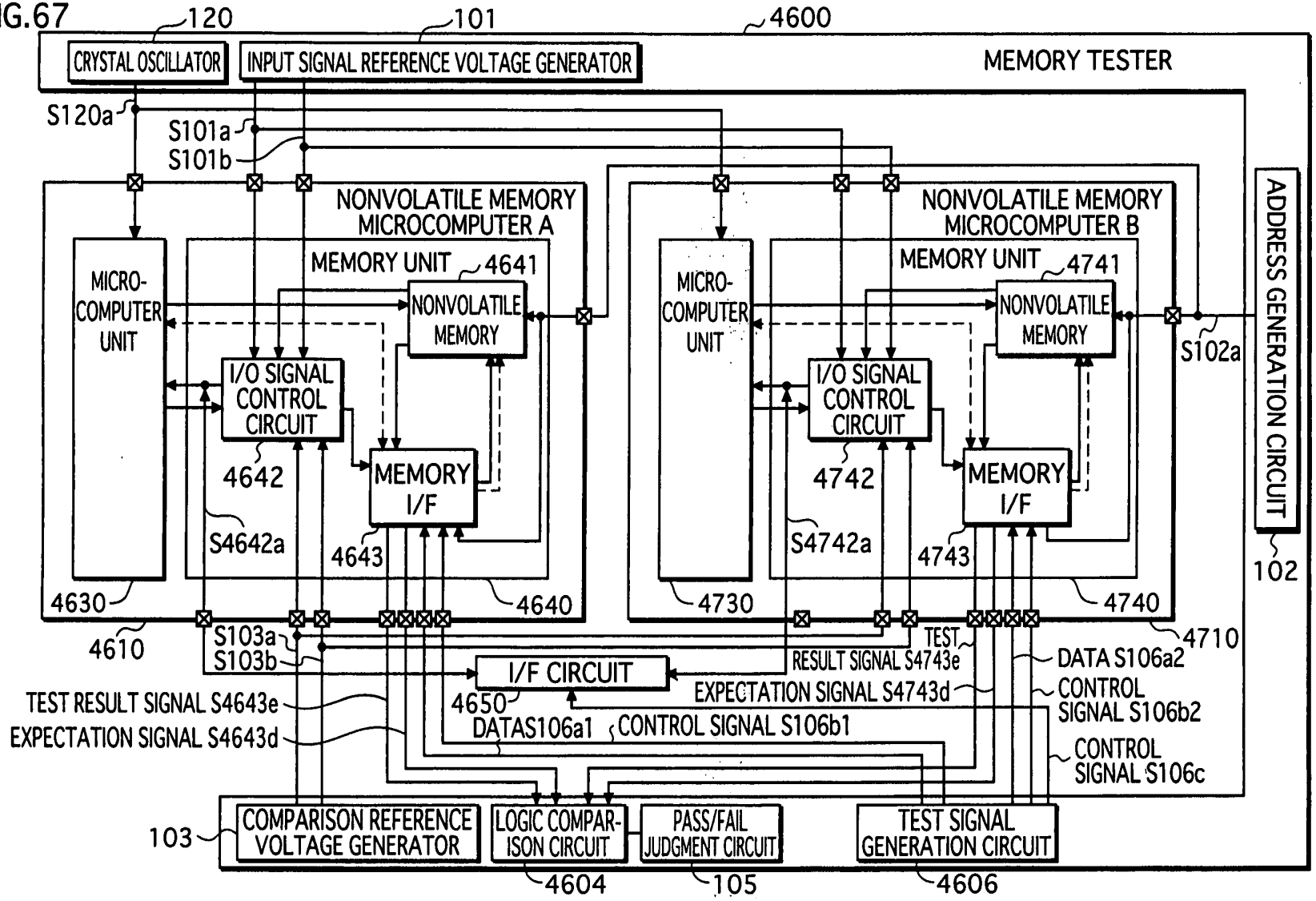

120
101
4600
CRYSTAL OSCILLATOR
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
MEMORY TESTER
S120a
S101a
S101b
NONVOLATILE MEMORY MICROCOMPUTER A
NONVOLATILE MEMORY MICROCOMPUTER B
MEMORY UNIT
4641
4741
MICRO-COMPUTER UNIT
NONVOLATILE MEMORY
I/O SIGNAL CONTROL CIRCUIT
MEMORY I/F
4642
4742
4643
4743
S4642a
S4742a
4630
4730
4640
4740
4610
4710
S102a
ADDRESS GENERATION CIRCUIT
102
S103a
S103b
I/F CIRCUIT
4650
TEST RESULT SIGNAL S4643e
EXPECTATION SIGNAL S4643d
TEST RESULT SIGNAL S4743e
EXPECTATION SIGNAL S4743d
DATA S106a2
CONTROL SIGNAL S106b2
DATAS106a1
CONTROL SIGNAL S106b1
CONTROL SIGNAL S106c
103
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPAR-ISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
4604
105
4606

FIG.69

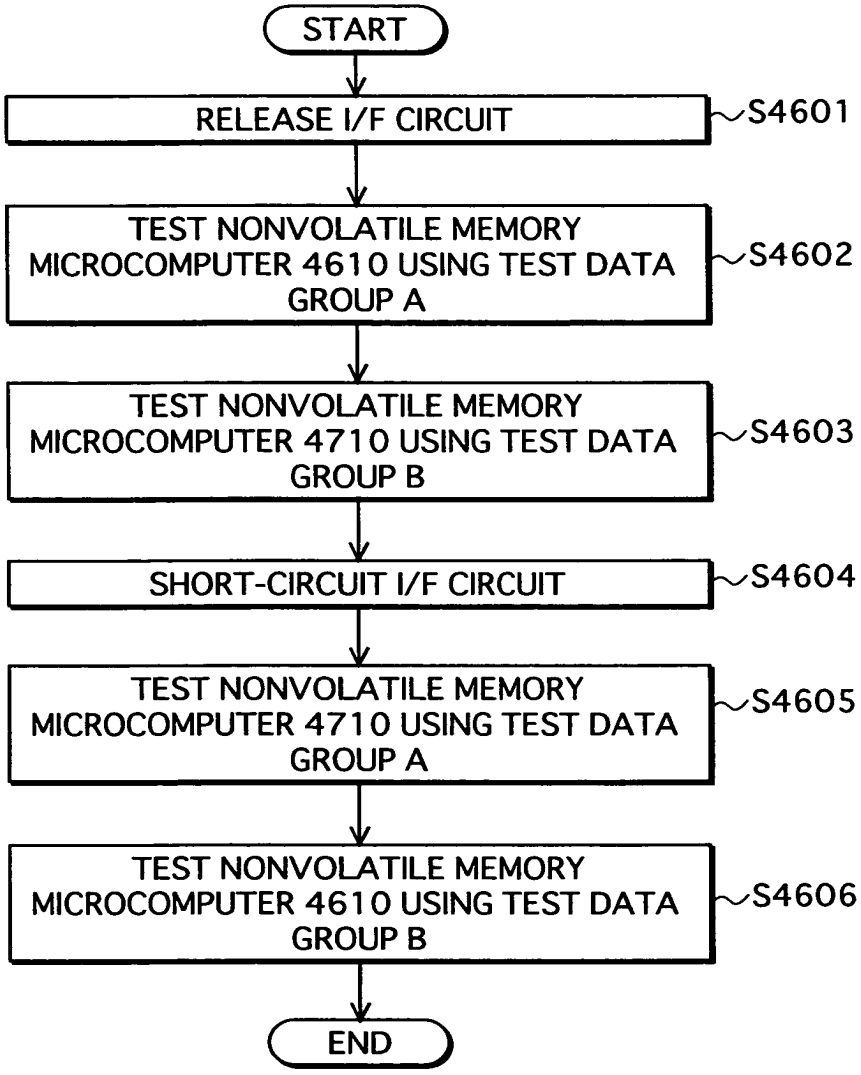

START
RELEASE I/F CIRCUIT
S4601
TEST NONVOLATILE MEMORY MICROCOMPUTER 4610 USING TEST DATA GROUP A
S4602
TEST NONVOLATILE MEMORY MICROCOMPUTER 4710 USING TEST DATA GROUP B
S4603
SHORT-CIRCUIT I/F CIRCUIT
S4604
TEST NONVOLATILE MEMORY MICROCOMPUTER 4710 USING TEST DATA GROUP A
S4605
TEST NONVOLATILE MEMORY MICROCOMPUTER 4610 USING TEST DATA GROUP B
S4606
END

FIG.70

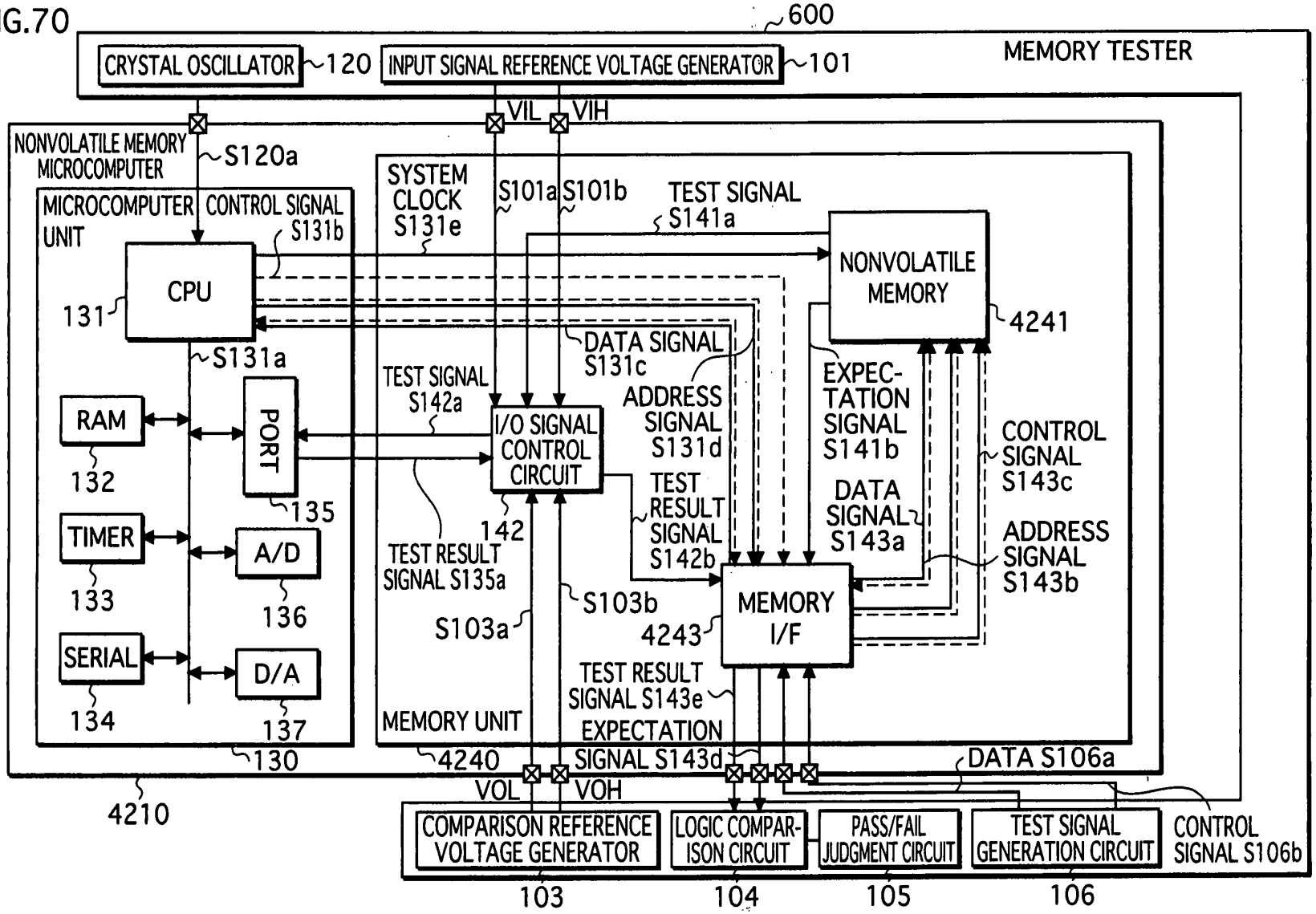

600
MEMORY TESTER
CRYSTAL OSCILLATOR
120
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
101
VIL
VIH
NONVOLATILE MEMORY MICROCOMPUTER
S120a
MICROCOMPUTER UNIT
CONTROL SIGNAL S131b
CPU
131
S131a
RAM
132
PORT
135
TIMER
133
A/D
136
SERIAL
134
D/A
137
130
4210
SYSTEM CLOCK S131e
S101a
S101b
TEST SIGNAL S141a
NONVOLATILE MEMORY
4241
DATA SIGNAL S131c
TEST SIGNAL S142a
ADDRESS SIGNAL S131d
EXPEC-TATION SIGNAL S141b
CONTROL SIGNAL S143c
I/O SIGNAL CONTROL CIRCUIT
142
TEST RESULT SIGNAL S142b
DATA SIGNAL S143a
ADDRESS SIGNAL S143b
TEST RESULT SIGNAL S135a
S103b
S103a
MEMORY I/F
4243
TEST RESULT SIGNAL S143e
MEMORY UNIT
EXPECTATION SIGNAL S143d
DATA S106a
4240
VOL
VOH
COMPARISON REFERENCE VOLTAGE GENERATOR
LOGIC COMPAR-ISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
CONTROL SIGNAL S106b
103
104
105
106

FIG.71

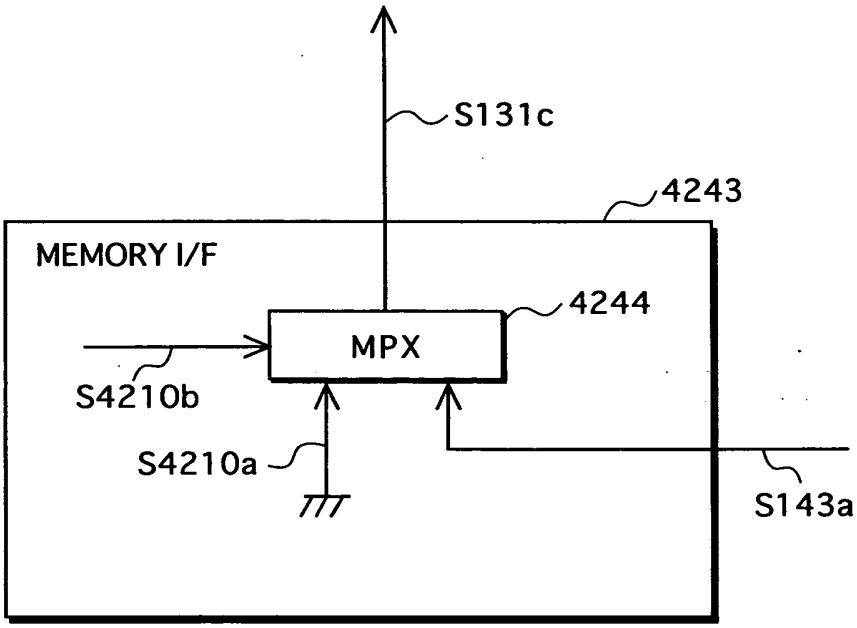
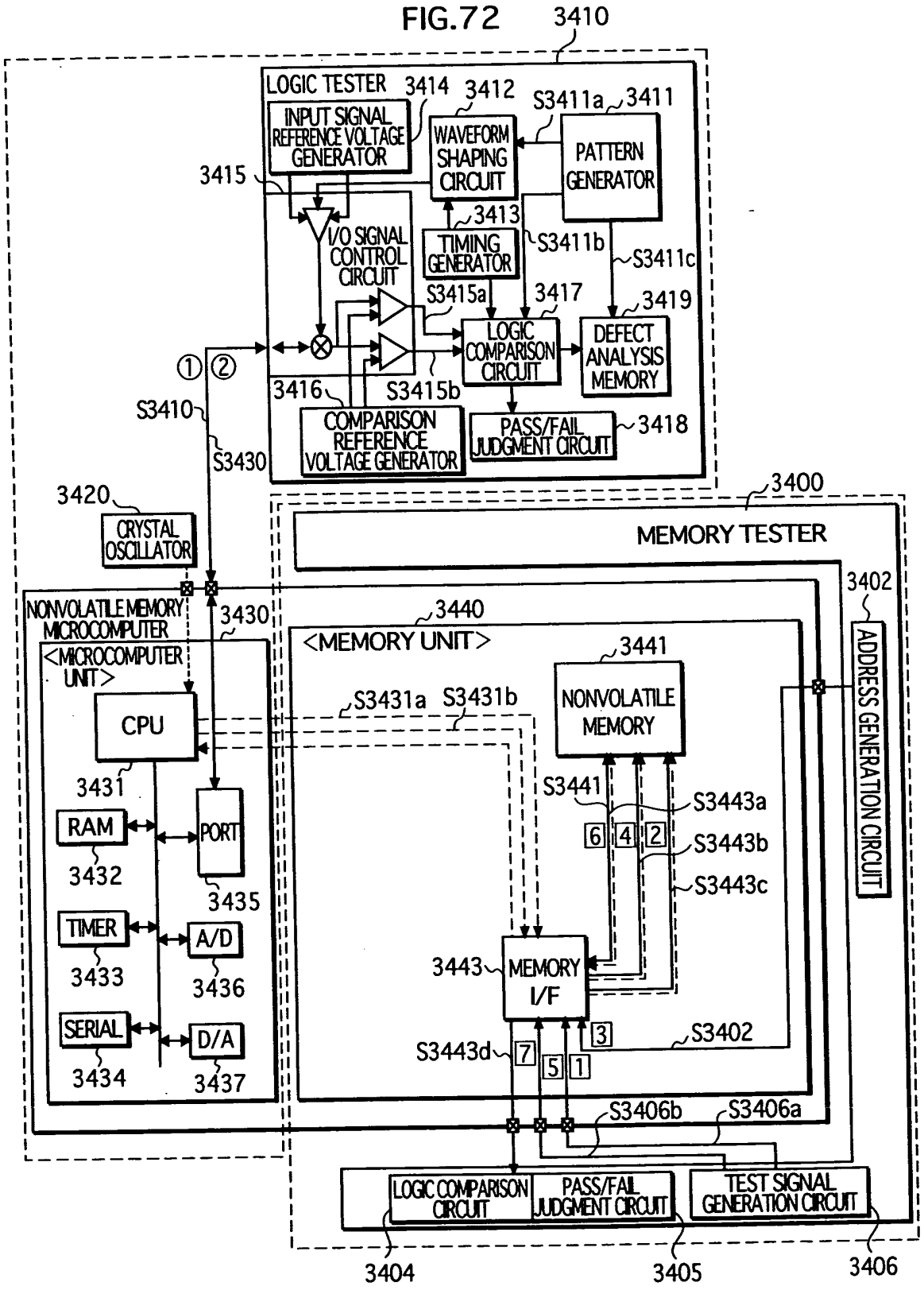


FIG.72


3410
LOGIC TESTER
3414
3412
S3411a
3411
INPUT SIGNAL REFERENCE VOLTAGE GENERATOR
WAVEFORM SHAPING CIRCUIT
PATTERN GENERATOR
3415
3413
I/O SIGNAL CONTROL CIRCUIT
TIMING GENERATOR
S3411b
S3411c
S3415a
3417
3419
LOGIC COMPARISON CIRCUIT
DEFECT ANALYSIS MEMORY
① ②
3416
S3415b
S3410
COMPARISON REFERENCE VOLTAGE GENERATOR
PASS/FAIL JUDGMENT CIRCUIT
3418
S3430
3420
CRYSTAL OSCILLATOR
3400
MEMORY TESTER
3402
NONVOLATILE MEMORY MICROCOMPUTER
3430
3440
<MEMORY UNIT>
<MICROCOMPUTER UNIT>
3441
S3431a
S3431b
NONVOLATILE MEMORY
CPU
3431
S3441
S3443a
6
4
2
S3443b
S3443c
RAM
PORT
3432
3435
TIMER
A/D
3433
3436
3443
MEMORY I/F
SERIAL
D/A
3434
3437
S3443d
7
5
1
3
S3402
ADDRESS GENERATION CIRCUIT
S3406b
S3406a
LOGIC COMPARISON CIRCUIT
PASS/FAIL JUDGMENT CIRCUIT
TEST SIGNAL GENERATION CIRCUIT
3404
3405
3406